Miniaturization and future prospects of Si devices

G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices: Prospects by World's Leading Scientists

October 4, 2011

Hiroshi Iwai,
Tokyo Institute of Technology

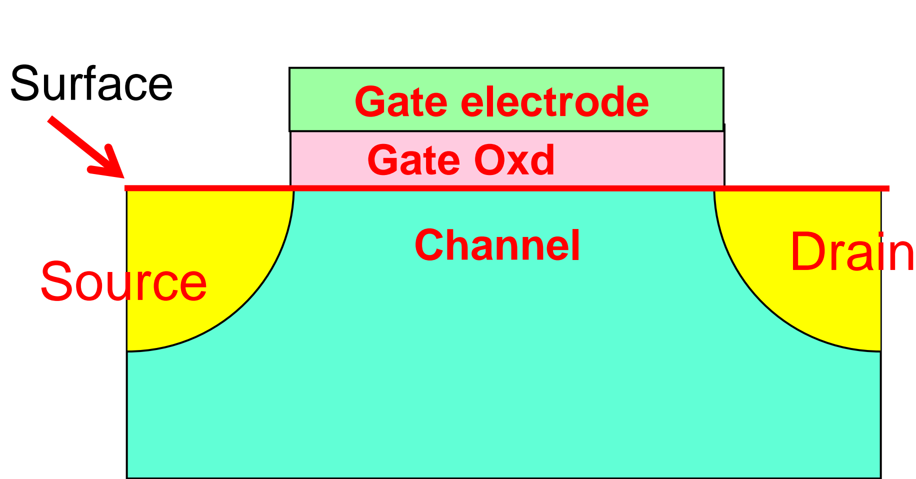
First Computer Eniac: made of huge number of vacuum tubes 1946

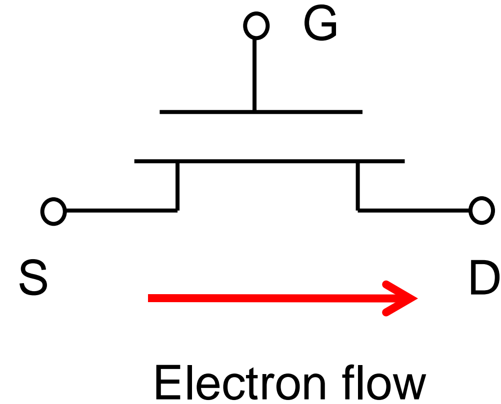
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

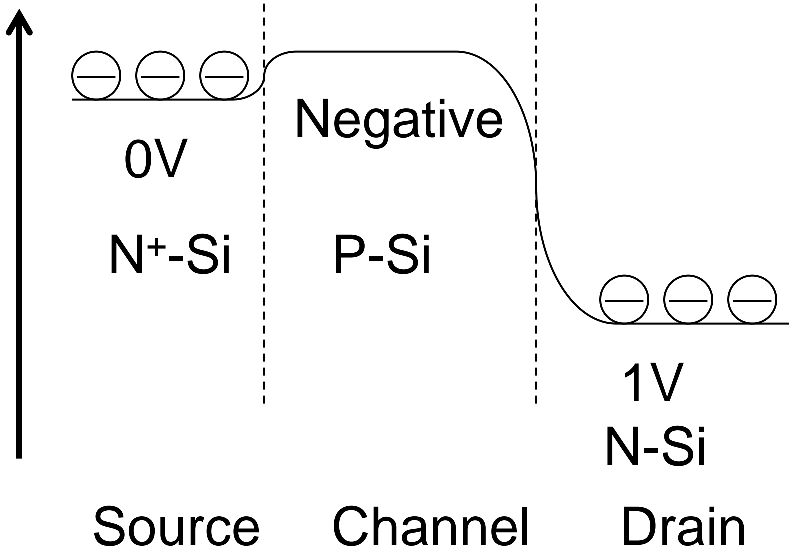
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

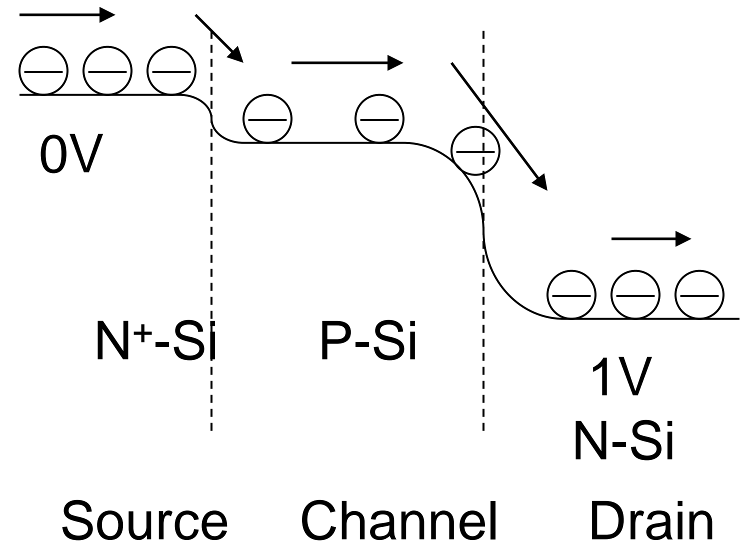




0 bias for gate

Positive bias for gate

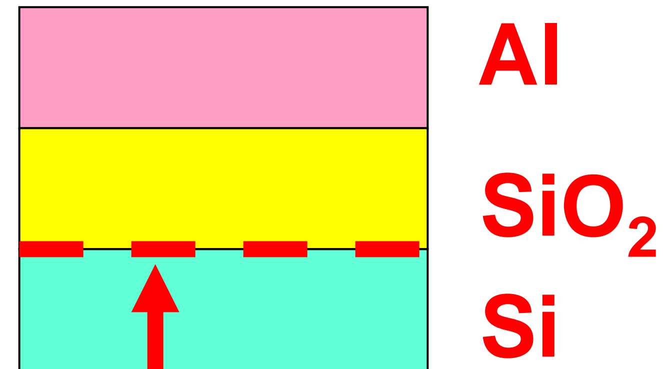




1960: First MOSFET by D. Kahng and M. Atalla

Top View

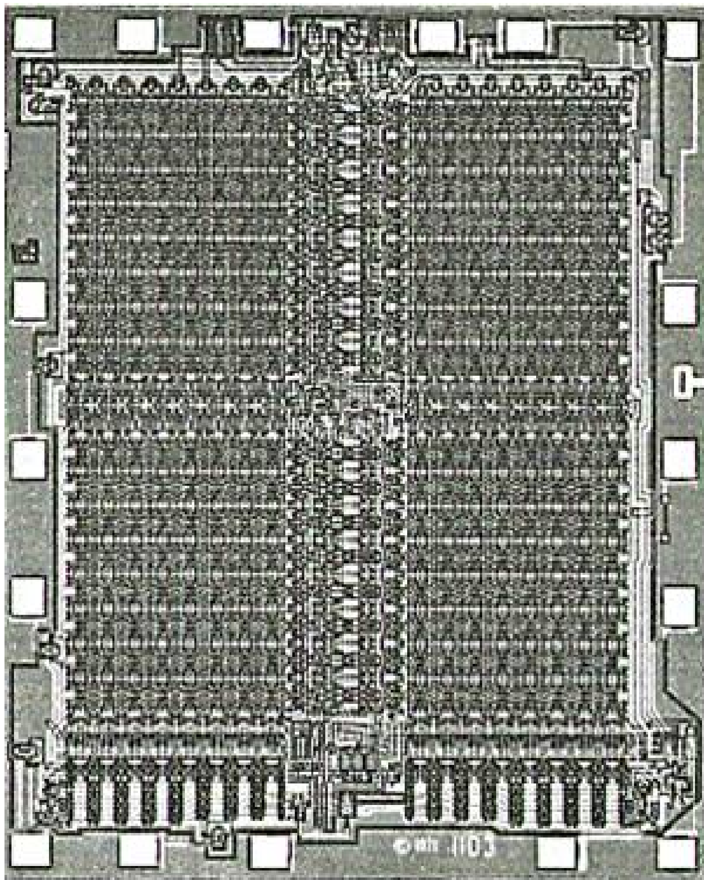
Si
Source
Al Gate
Drain
Si

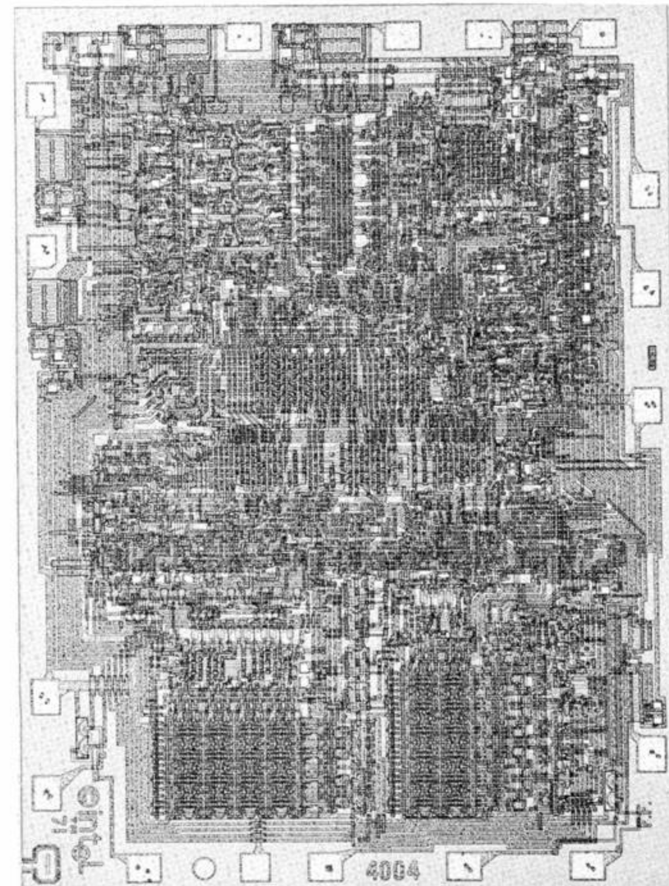


Si/SiO_2 Interface is exceptionally good

1970,71: 1st generation of LSIs

1kbit DRAM Intel 1103 **4bit MPU Intel 4004**





2011

Most recent SD Card

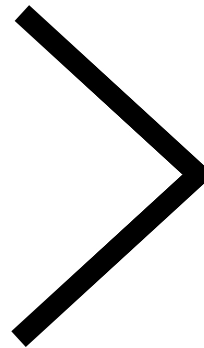
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population：6 Billion
Brain Cell：10～100 Billion
Stars in Galaxy：100 Billion

Most Recent SD Card



2.4cm X 3.2cm X 0.21cm

Volume：1. 6cm³ Weight：2g

Voltage：2.7 - 3.6V

Old Vacuum Tube：
5cm X 5cm X 10cm, 100g,100W

1Tbit = 10k X10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km^3 = $0.25X10^{12}cm^3$

Weight = 0.1 $kgX10^{12}$ = $0.1X10^9$ton = 100 M ton

Power = $0.1kWX10^{12}$=50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW

So, progress of IC technology is most important for the power saving!

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Transistor Scaling Continues

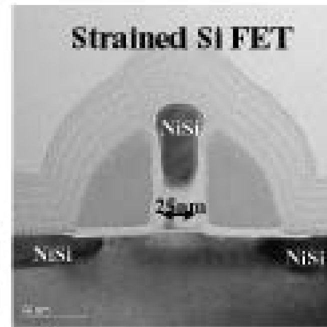
90nm node

Lg=50nm

65nm node

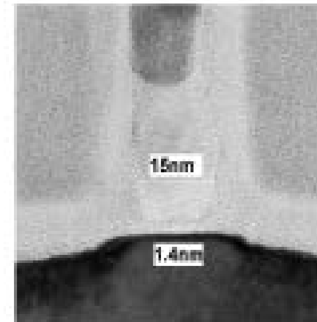
Lg=35nm

45nm node



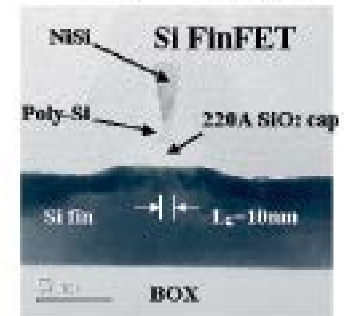
Lg=25nm

32nm node

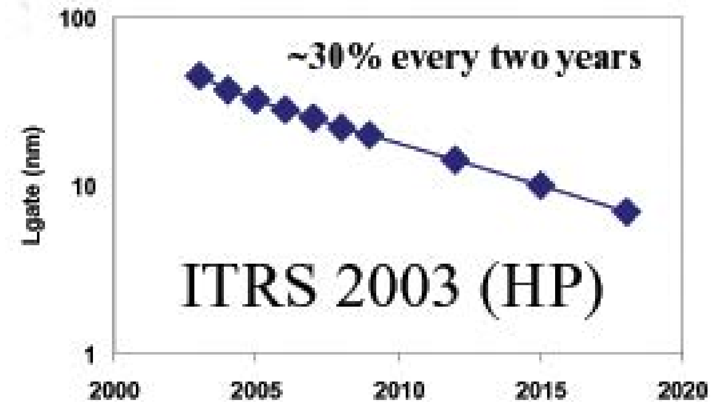


Lg=15nm

22nm node



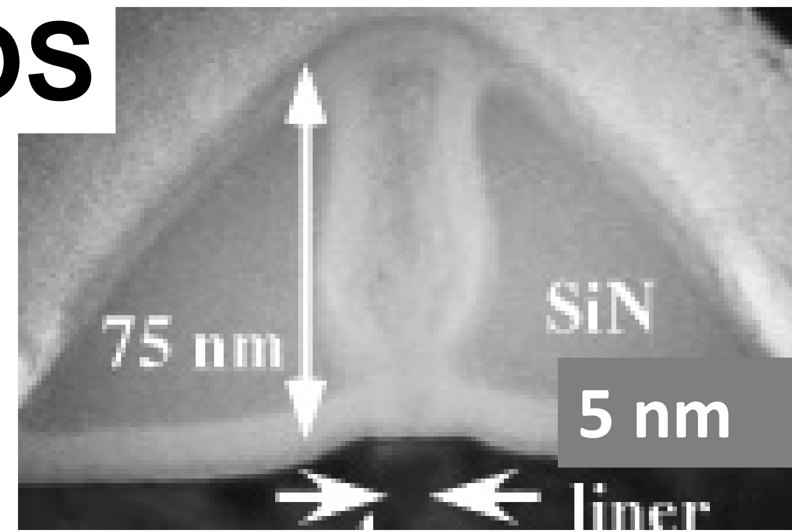
Lg=10nm



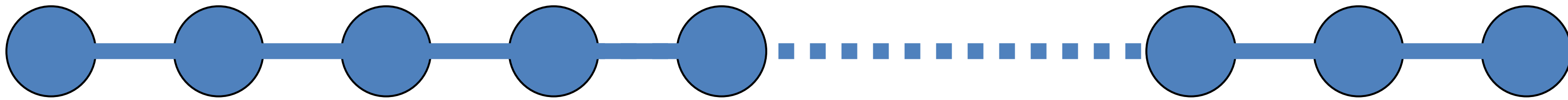
Qi Xinag, ECS 2004, AMD

5 nm gate length CMOS

Is a Real Nano Device!!

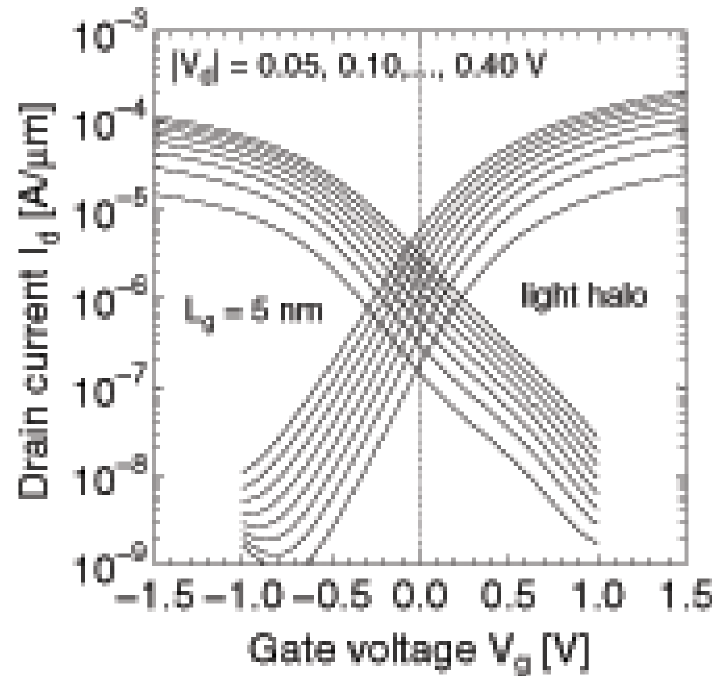


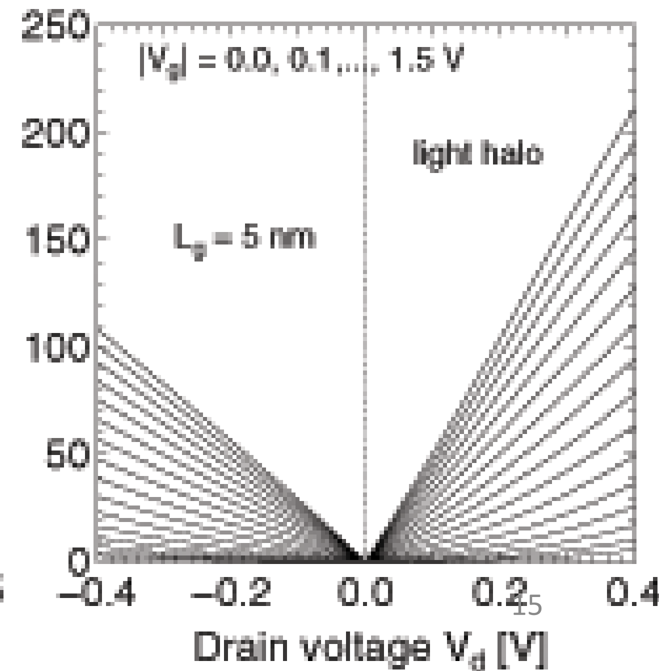
Length of 18 Si atoms

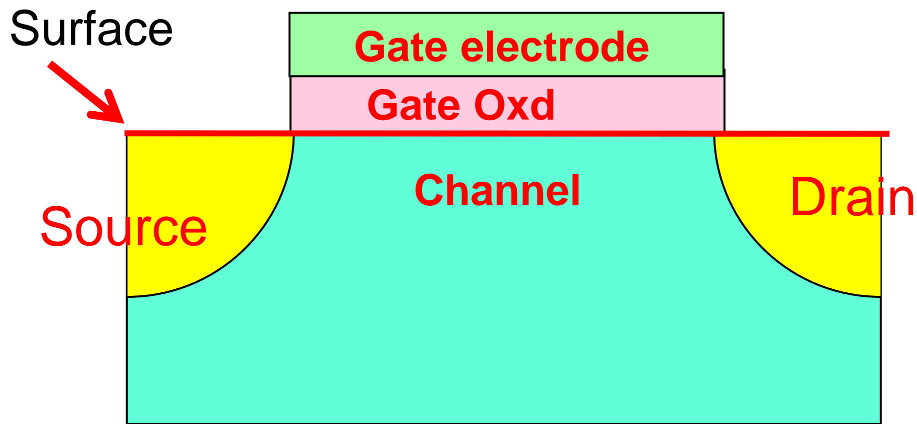


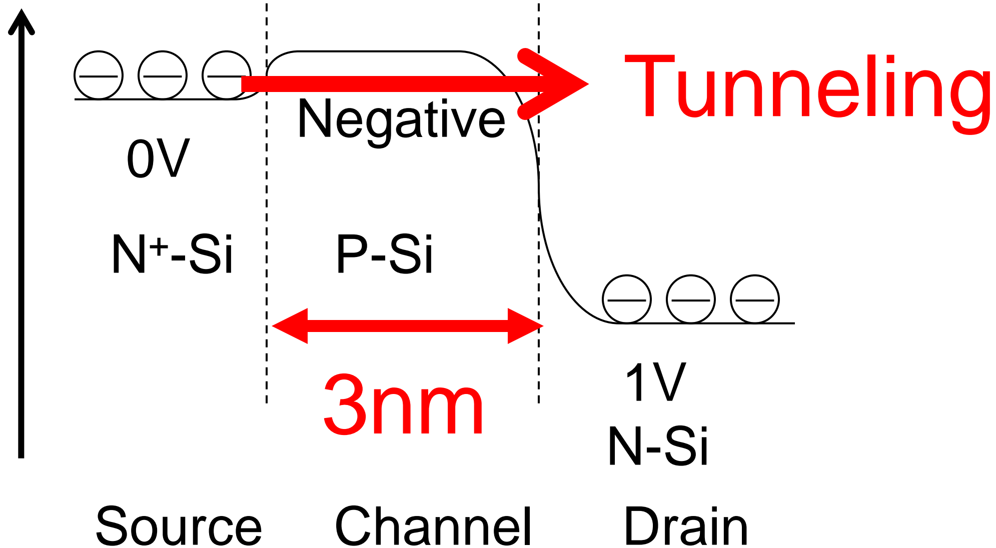
H. Wakabayashi et.al, NEC

IEDM, 2003







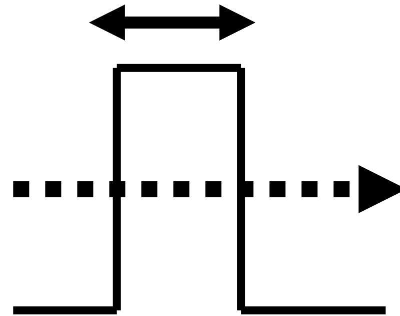


@Vg=0V,
Transistor cannot be switched off

Prediction now!

Limitation for MOSFET operation

Tunneling distance



3 nm

Lg = Sub-3 nm?

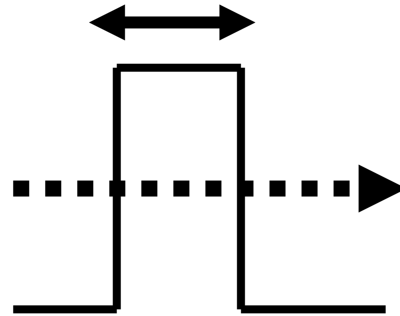
Below this, no one knows future!

Prediction now!

Limitation for MOSFET operation

Tunneling distance

3 nm



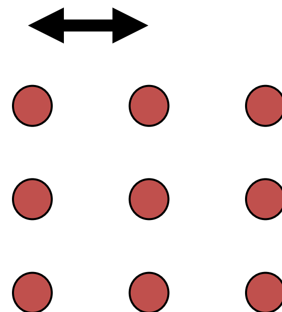
Lg = Sub-3 nm?

Below this, no one knows future!

Ultimate limitation

Atom distance

0.3 nm



No one can make a MOSET below this size!

Question:

How far we can go with downscaling?

How far can we go for production?

Past

0.7 times per 3 years

In 40 years: 18 generations, Size 1/300, Area 1/100,000

Now

1970年

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

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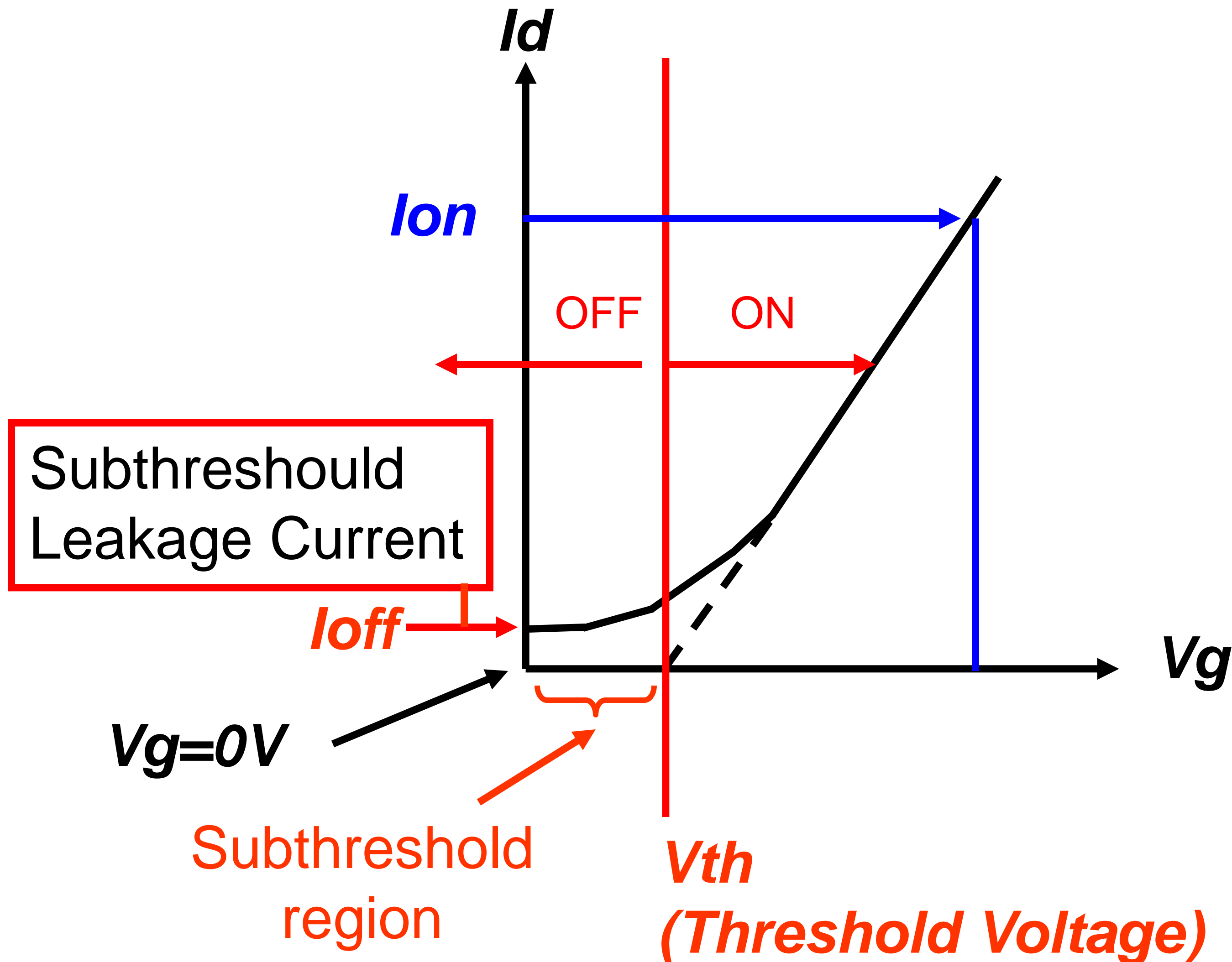
Future

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- **At least 4,5 generations to 8nm**
- **Hopefully 8 generations to 3nm**

Subtheshold leakage current of MOSFET



Log scale Id plot

Vth cannot be decreased anymore

↑

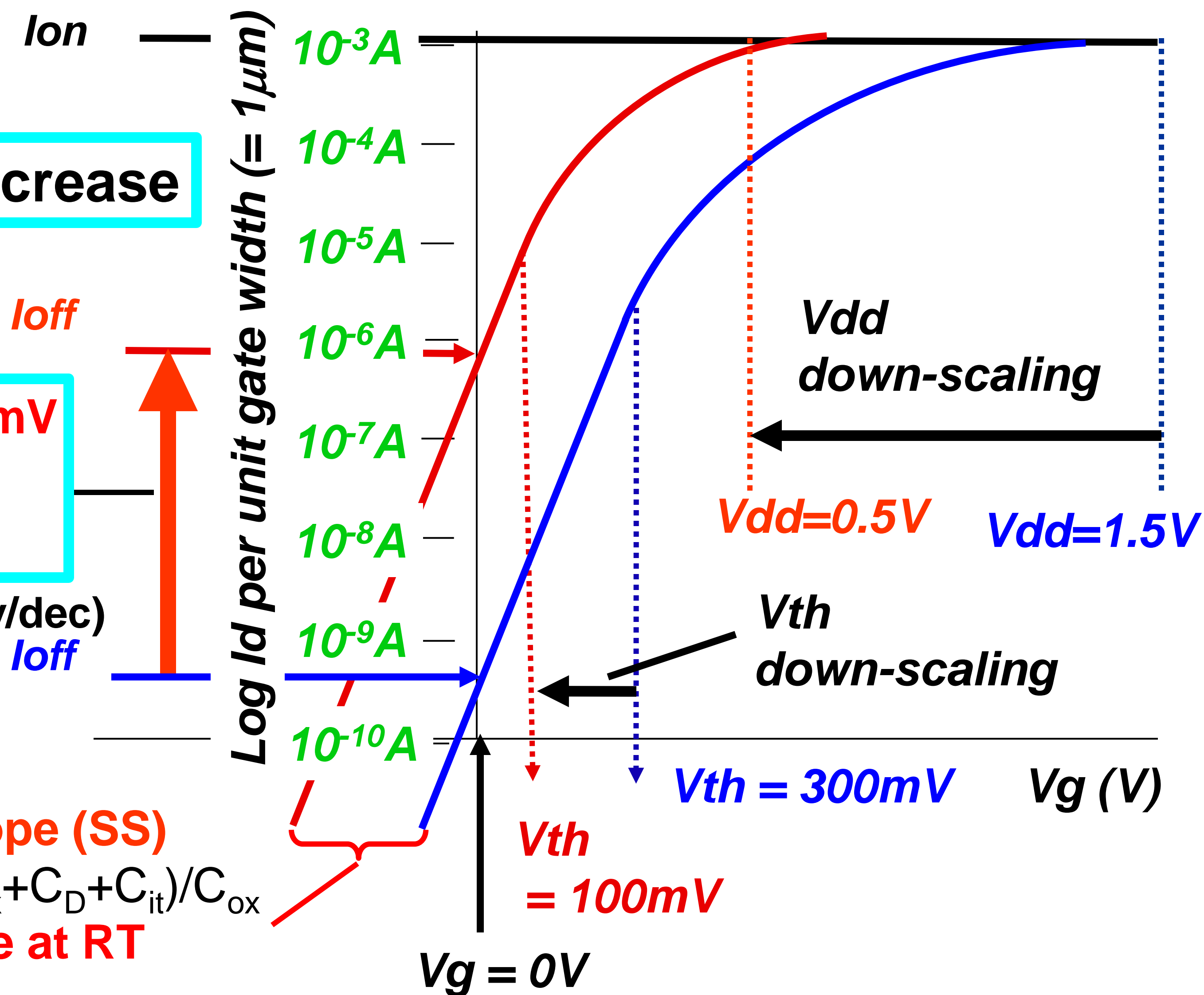
significant Ioff increase

↑

Vth: 300mV → 100mV

Ioff increases with 3.3 decades

(300 – 100)mV/(60mv/dec) = 3.3 dec



Subthreshold slope (SS)

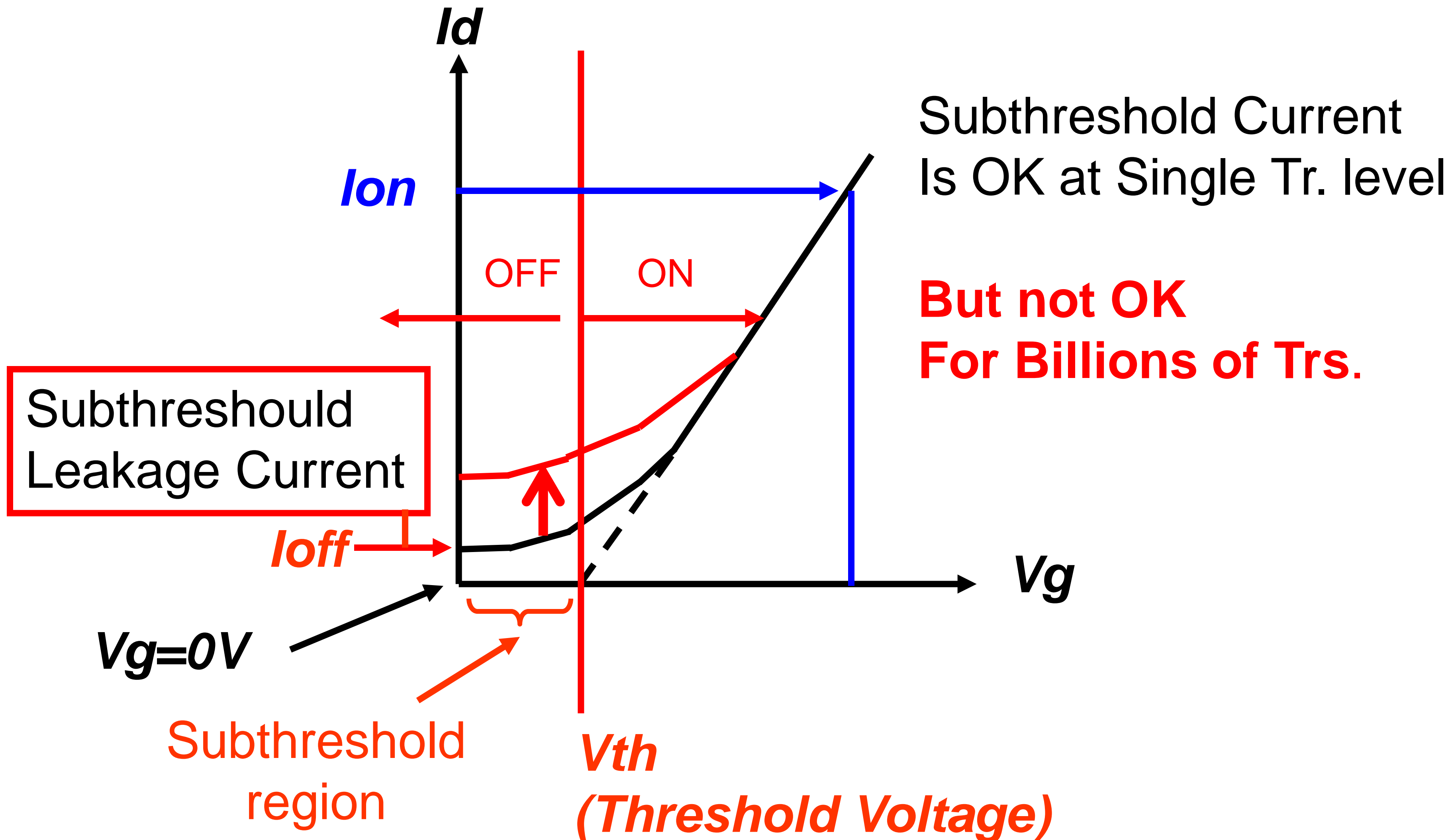
$= (\mathrm{Ln}10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}$

> ~ 60 mV/decade at RT

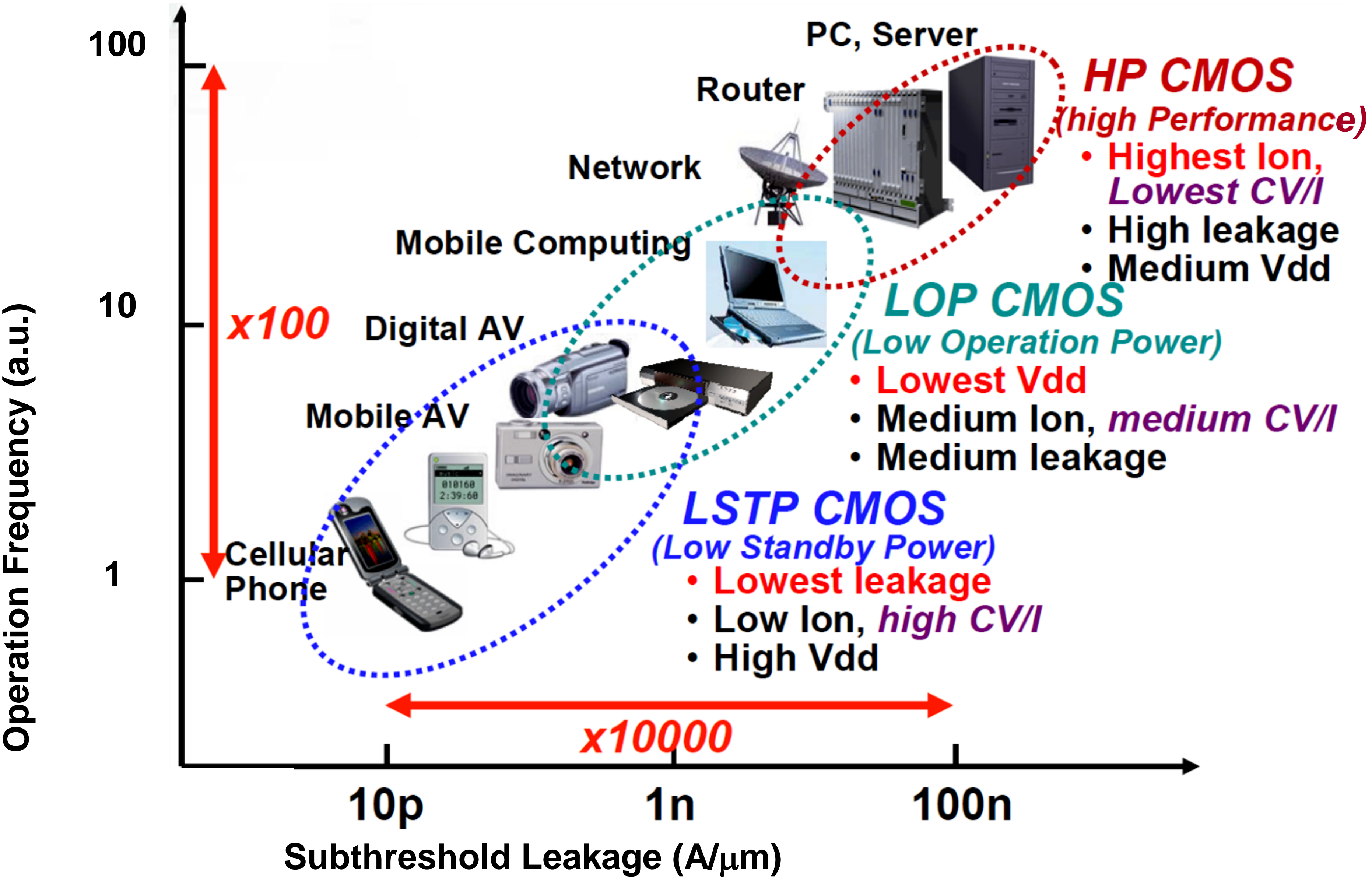
SS value:

Constant and does not become small with down-scaling

Subtheshold leakage current of MOSFET

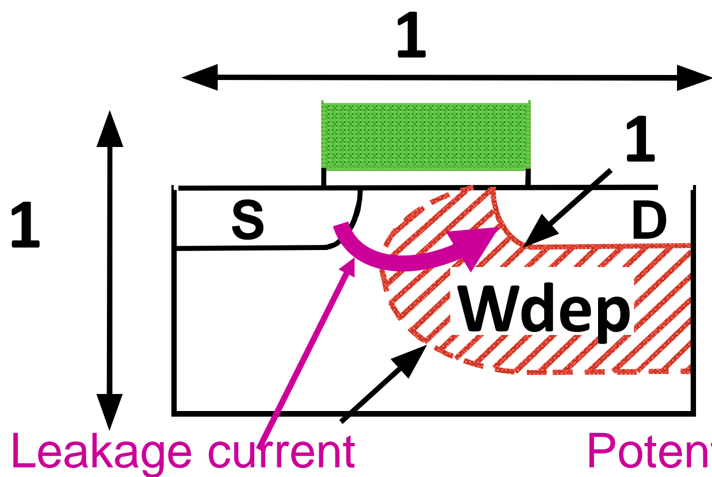


The limit is deferent depending on application



Source: 2007 ITRS Winter Public Conf.

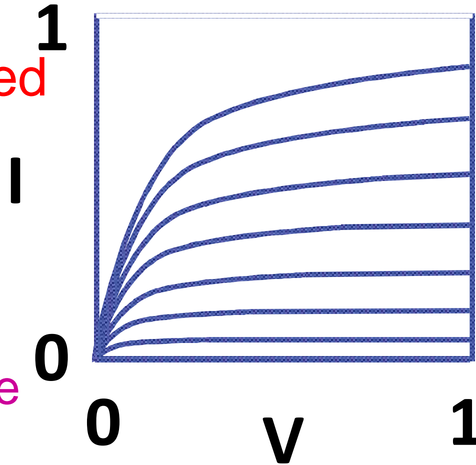
Scaling Method: by R. Dennard in 1974



Leakage current

Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



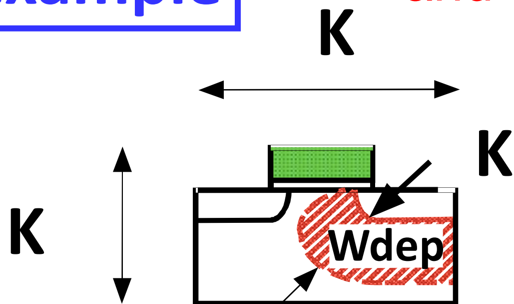
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

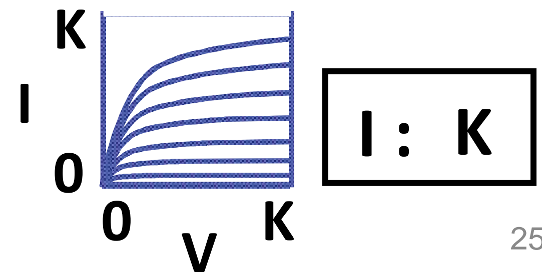
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$
$$: \quad K$$



I : K

Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

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3 important technological items for DS.

New materials

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D

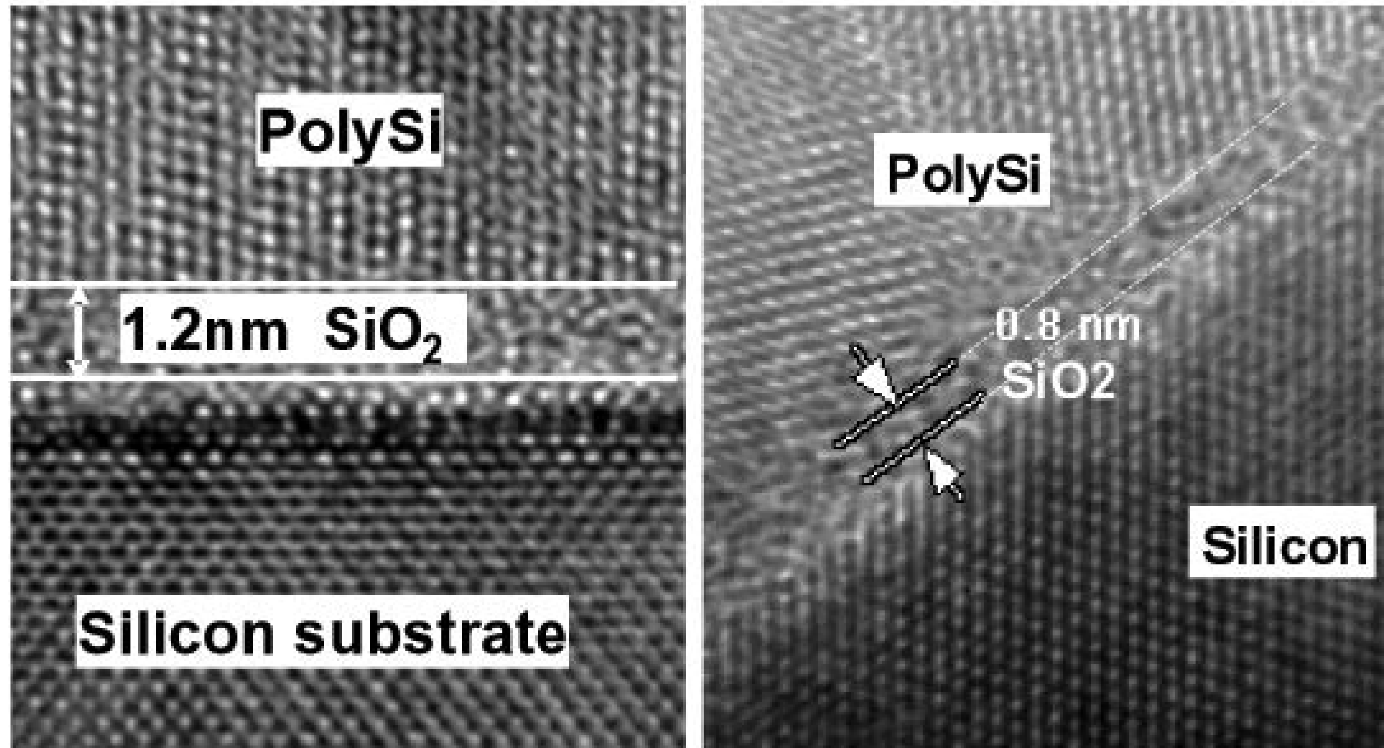
New structures

3. Wire channel

1. High-k beyond 0.5 nm

0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

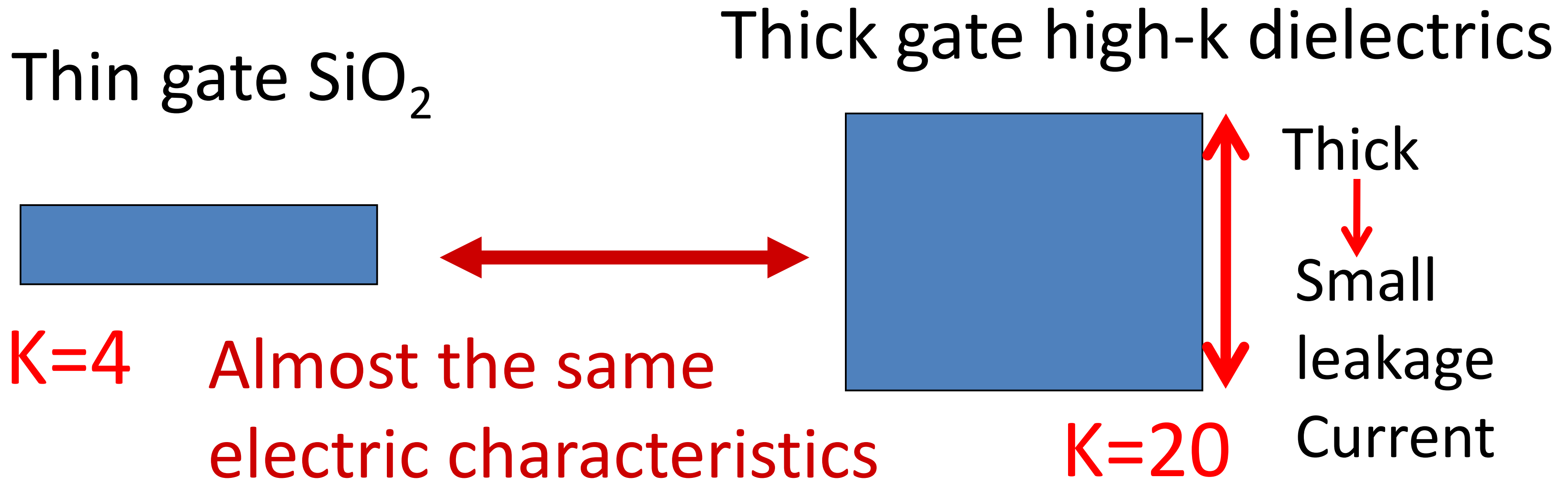


- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

There is a solution! K: Dielectric Constant

To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

Candidates ■

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
● H																	● He
Li	Be											● B	● C	● N	● O	● F	● Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	★	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

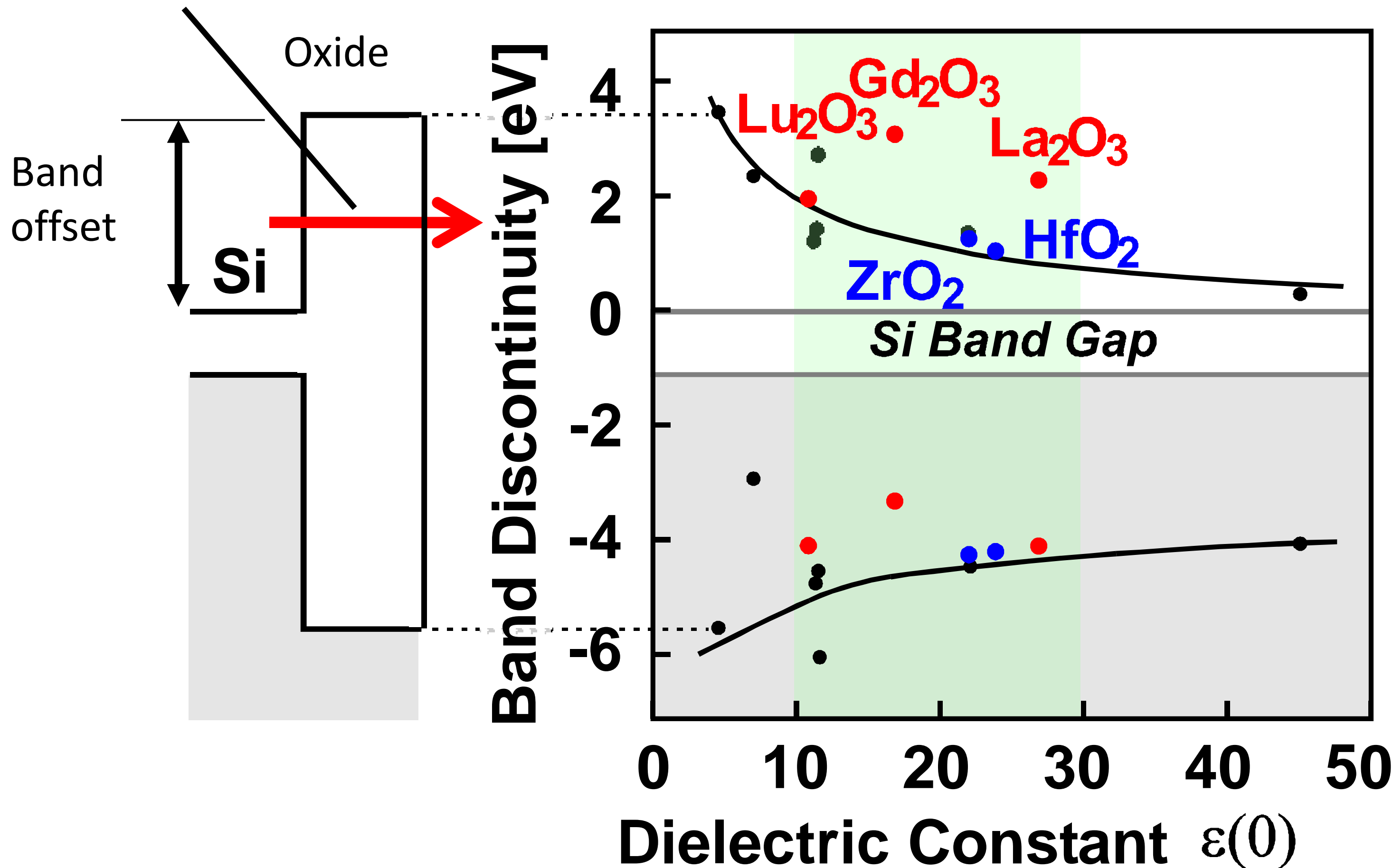
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

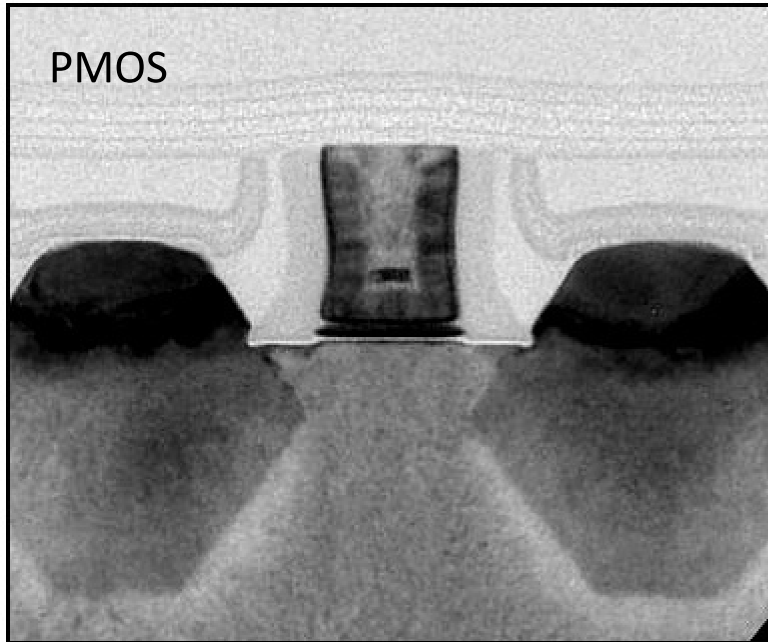
Conduction band offset vs. Dielectric Constant

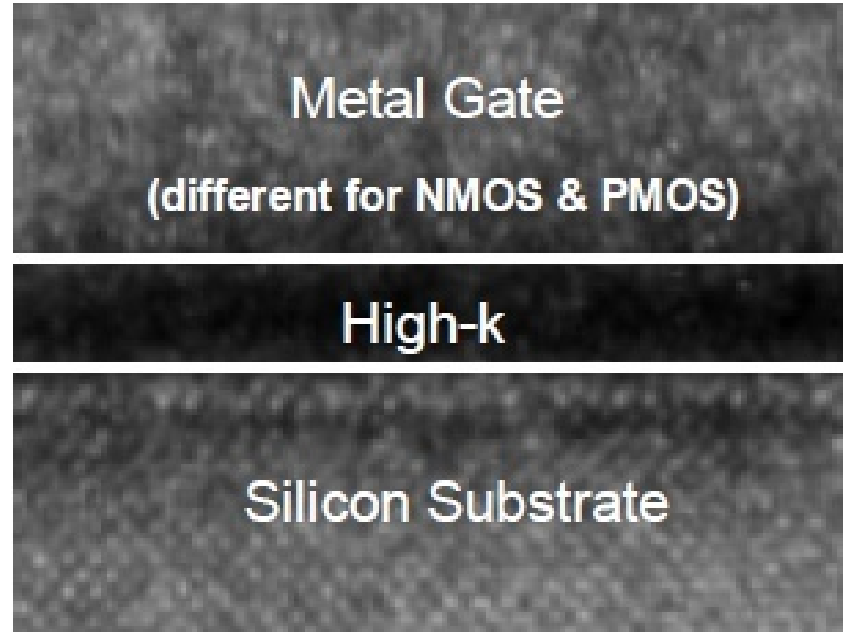


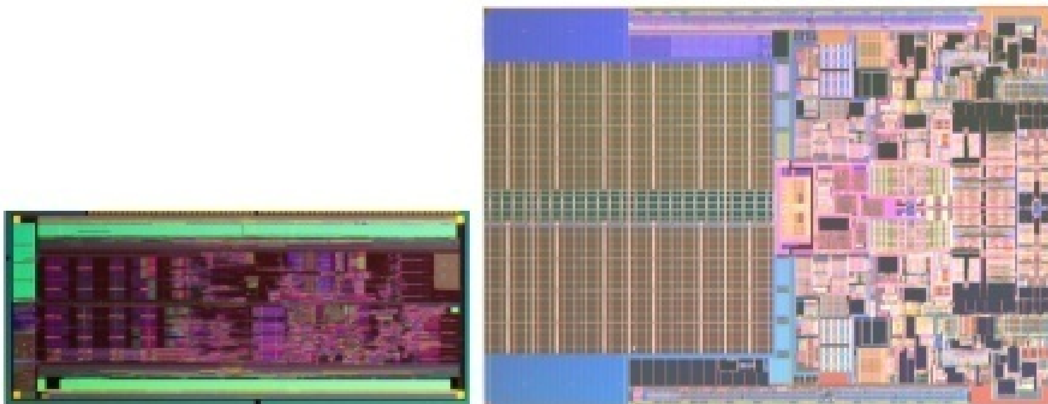
XPS measurement by Prof. T. Hattori, INFOS 2003

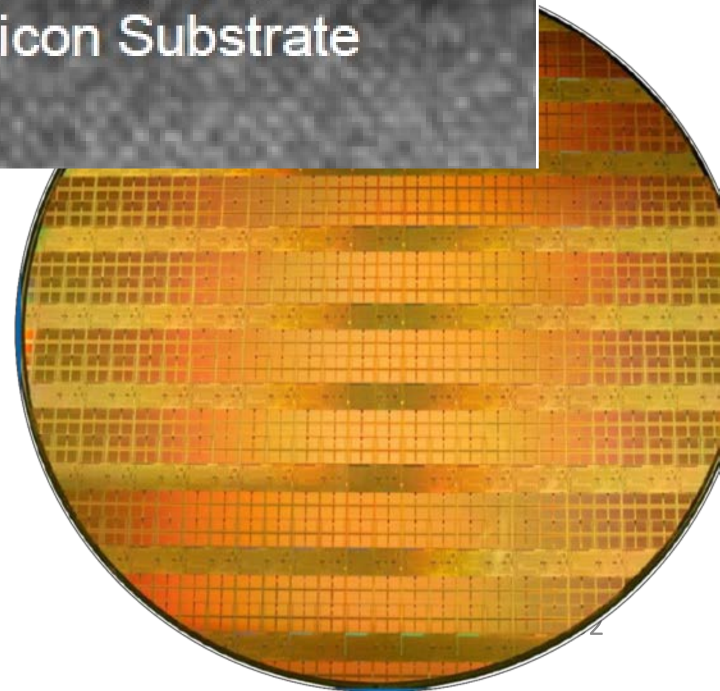
High-k gate insulator MOSFETs for Intel: EOT=1nm

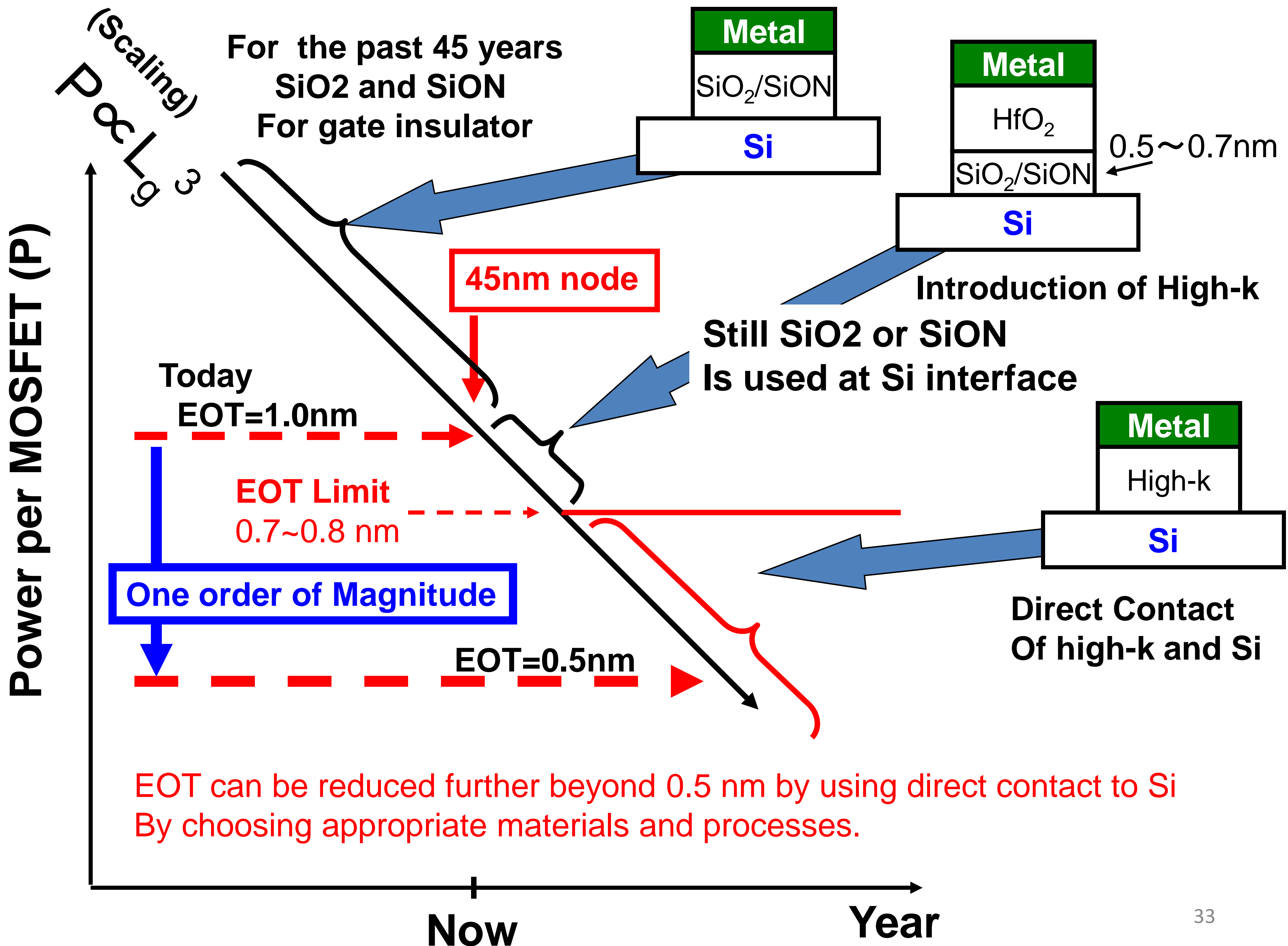
HfO_2 based high-k



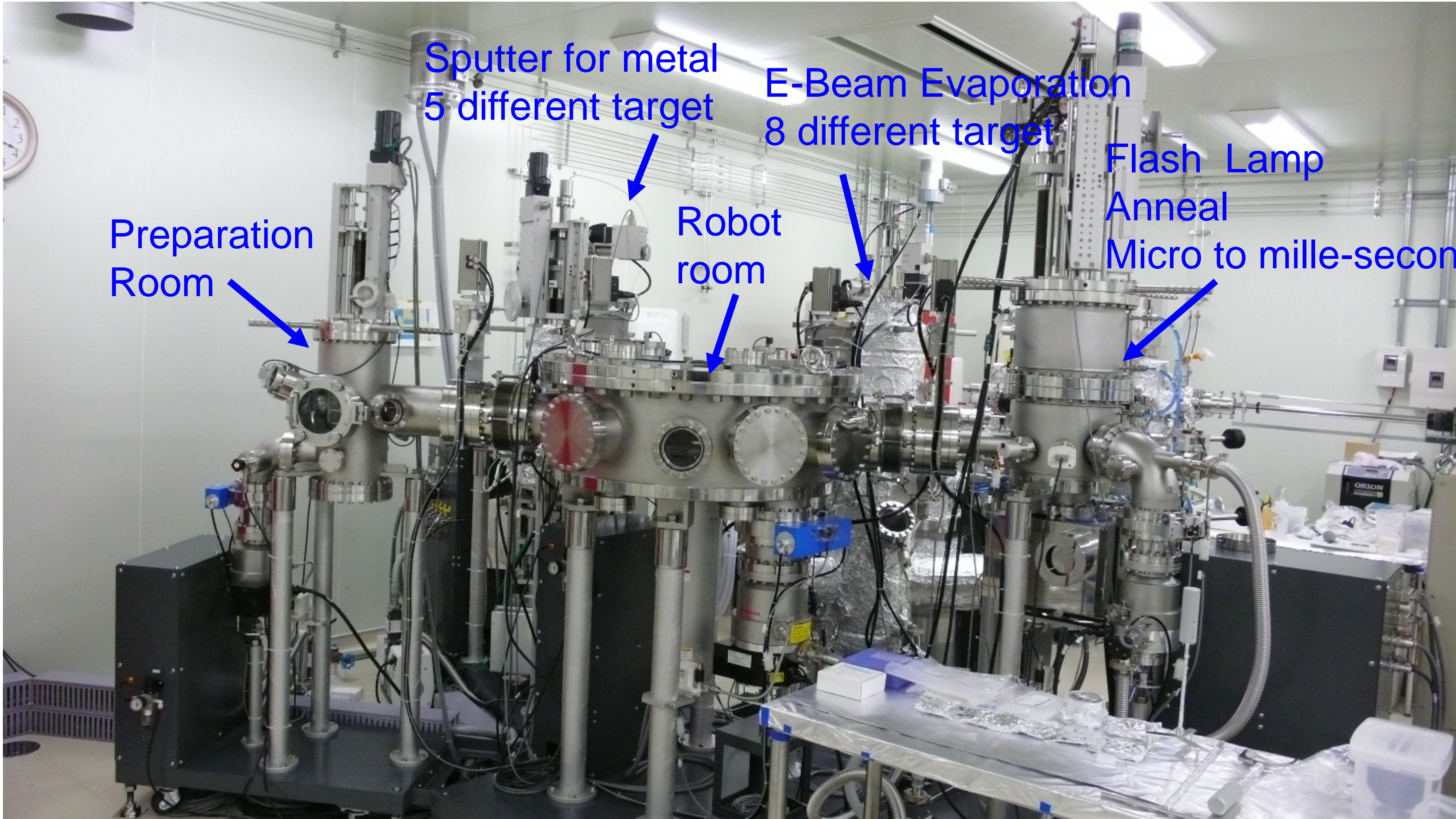




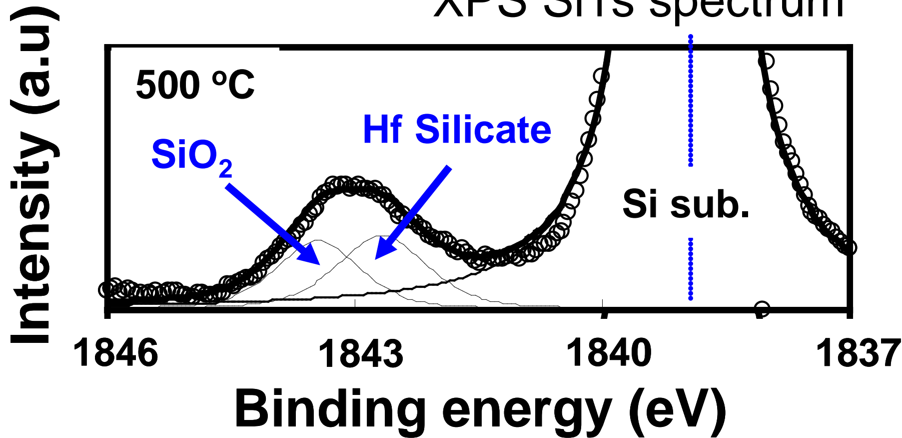


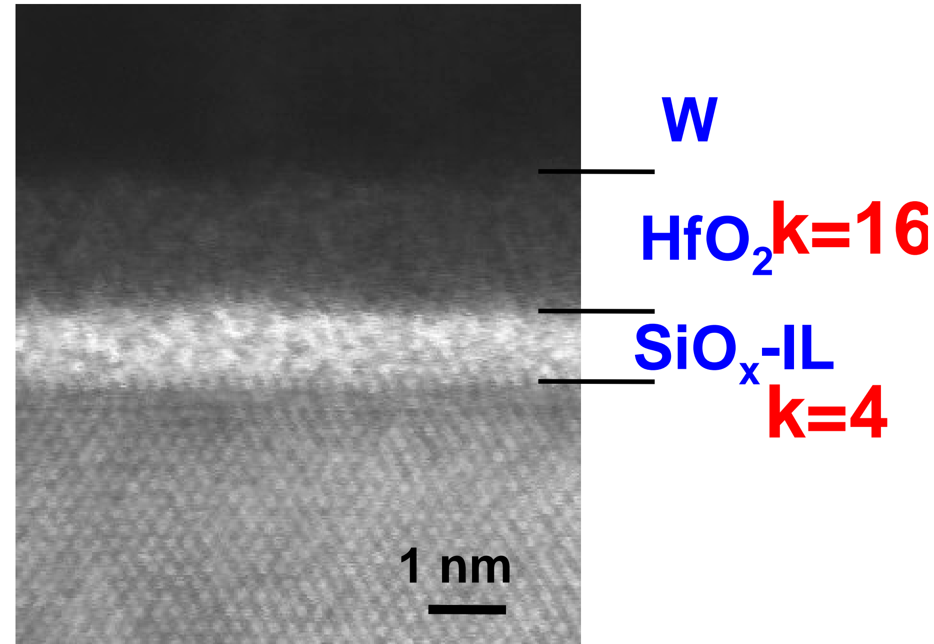

(Scaling)
P ∝ Lg 3
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
SiO2/SiON
Si
0.5～0.7nm
Introduction of High-k
45nm node
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
Metal
High-k
Si
One order of Magnitude
EOT=0.5nm
Direct Contact
Of high-k and Si
Power per MOSFET (P)
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.
Now
Year

Cluster tool for high-k thin film deposition

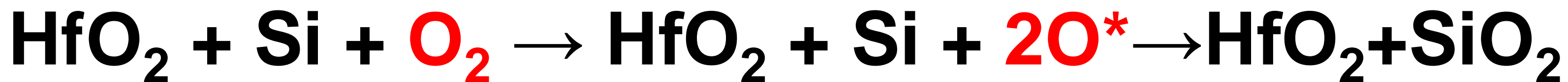


SiO_x-IL growth at HfO_2/Si Interface



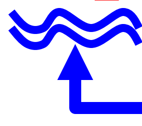


Phase separator



$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

La-Silicate Reaction at La_2O_3/Si

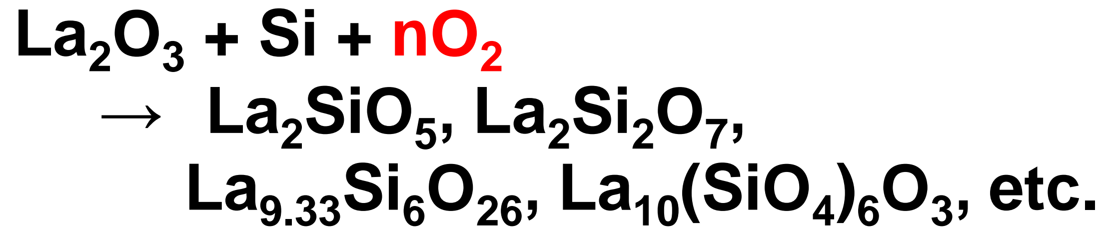
Direct contact high-k/Si is possible

XPS Si1s spectra

as depo.
La-silicate
Si sub.
300 ºC
500 ºC
Intensity (a.u)
1846 1843 1840 1837
Binding energy (eV)

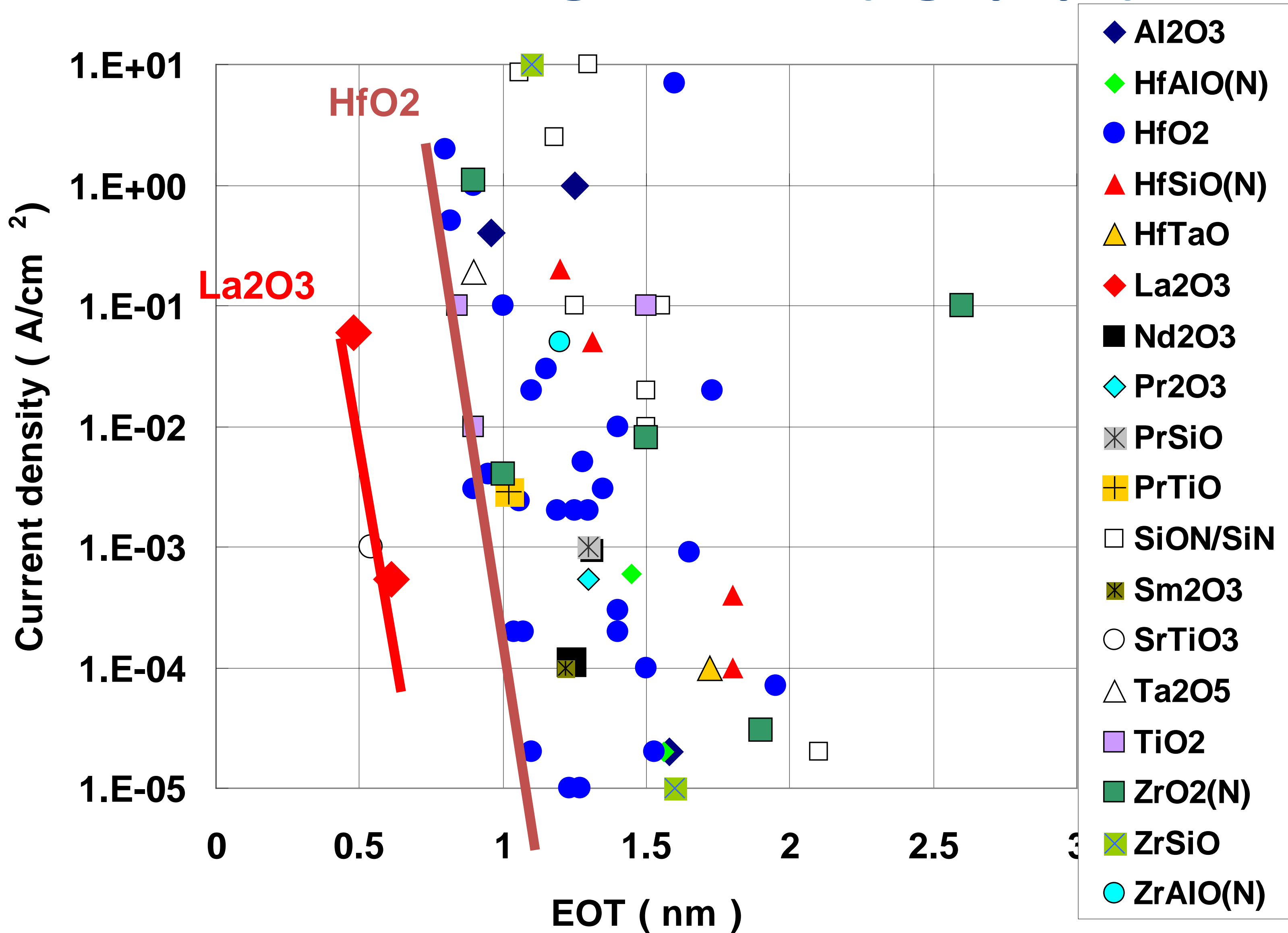
TEM image **500 ºC, 30 min**

W
La_2O_3 k=23
La-silicate k=8~14
1 nm



La_2O_3 can achieve direct contact of high-k/Si

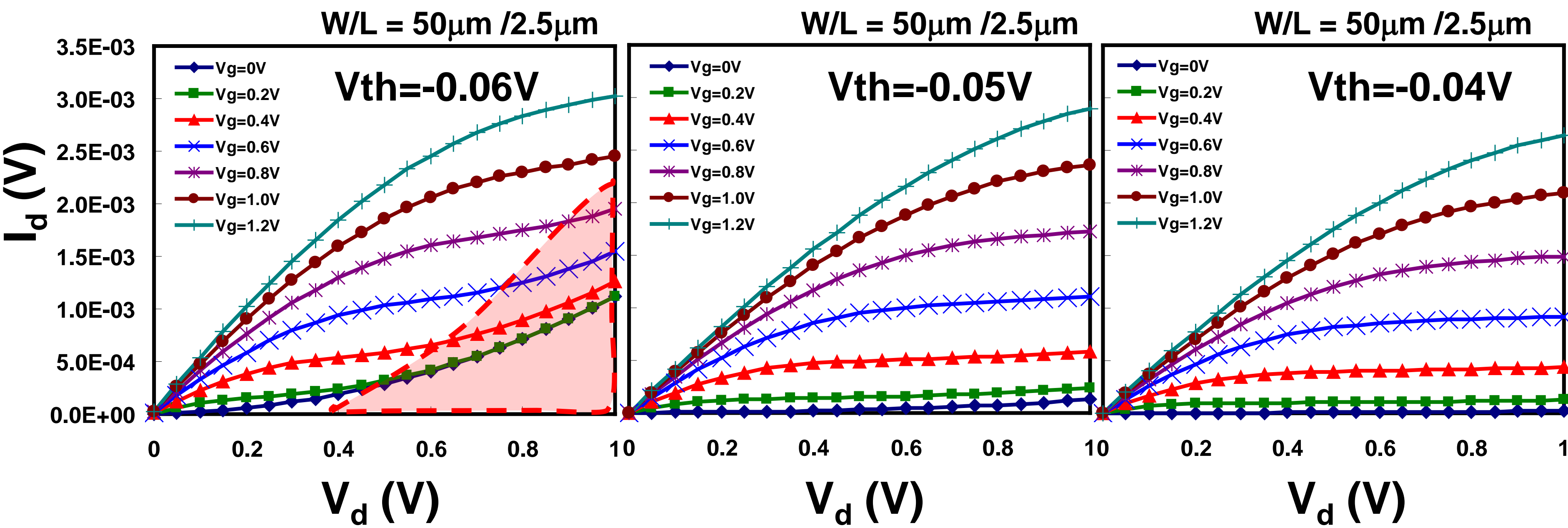
Gate Leakage vs EOT, (Vg=|1|V)



La_2O_3 at 300ºC process make sub-0.4 nm EOT MOSFET

EOT=0.37nm

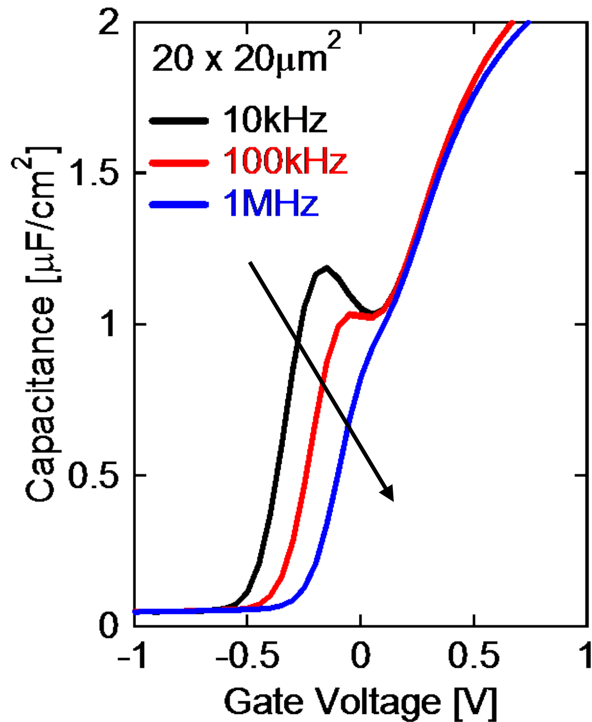
EOT=0.37nm EOT=0.40nm EOT=0.48nm



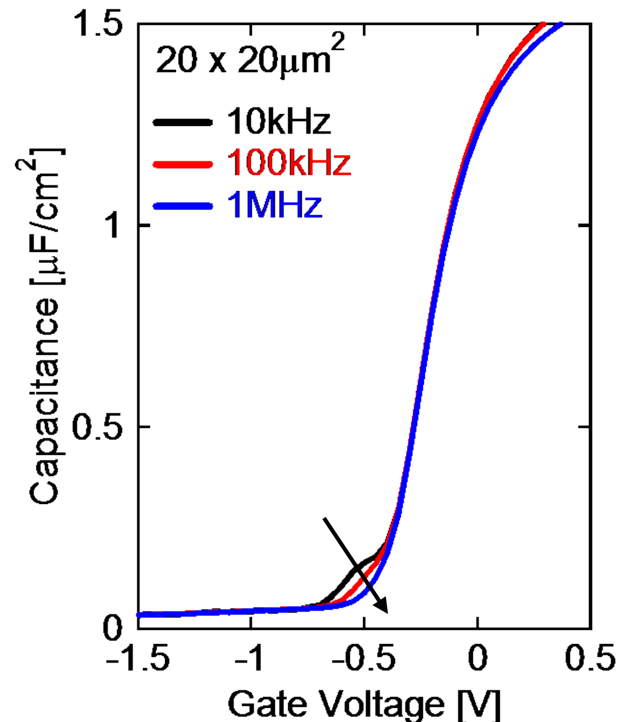
0.48 →0.37nm Increase of Id at 30%

However, high-temperature anneal is necessary for the good interfacial property

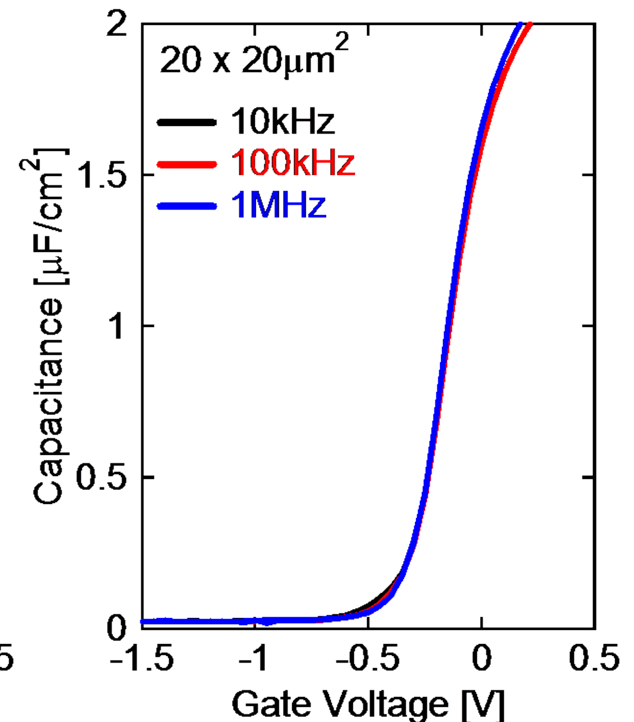
FGA500^{o}C 30min



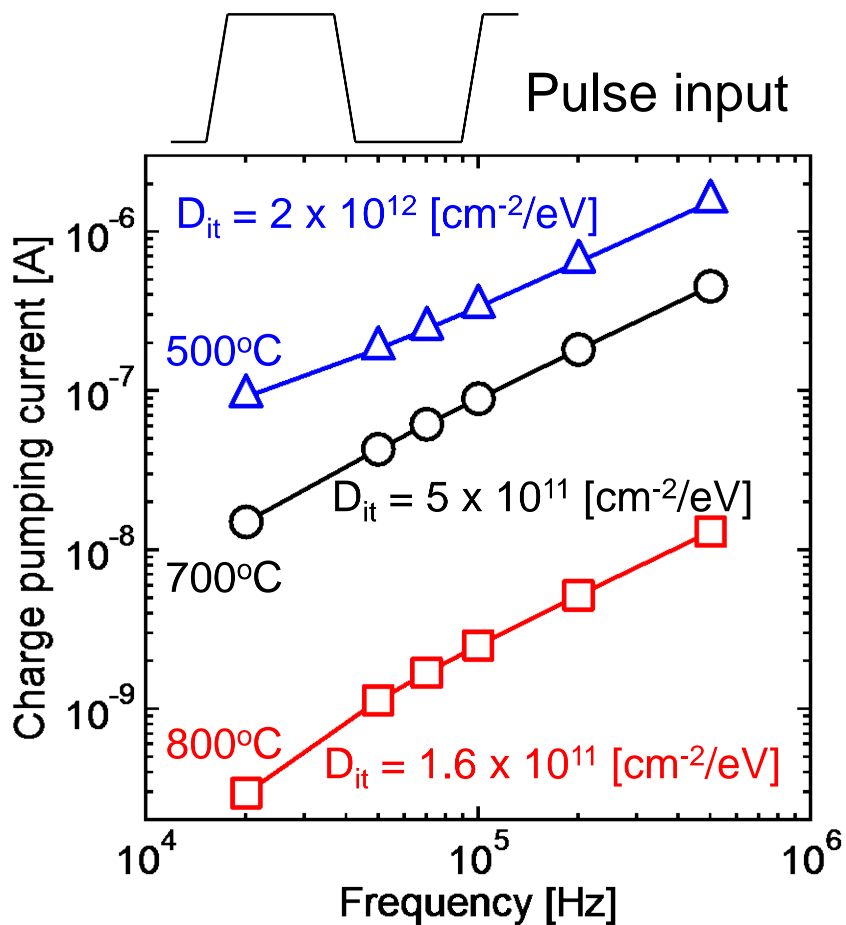
FGA700^{o}C 30min

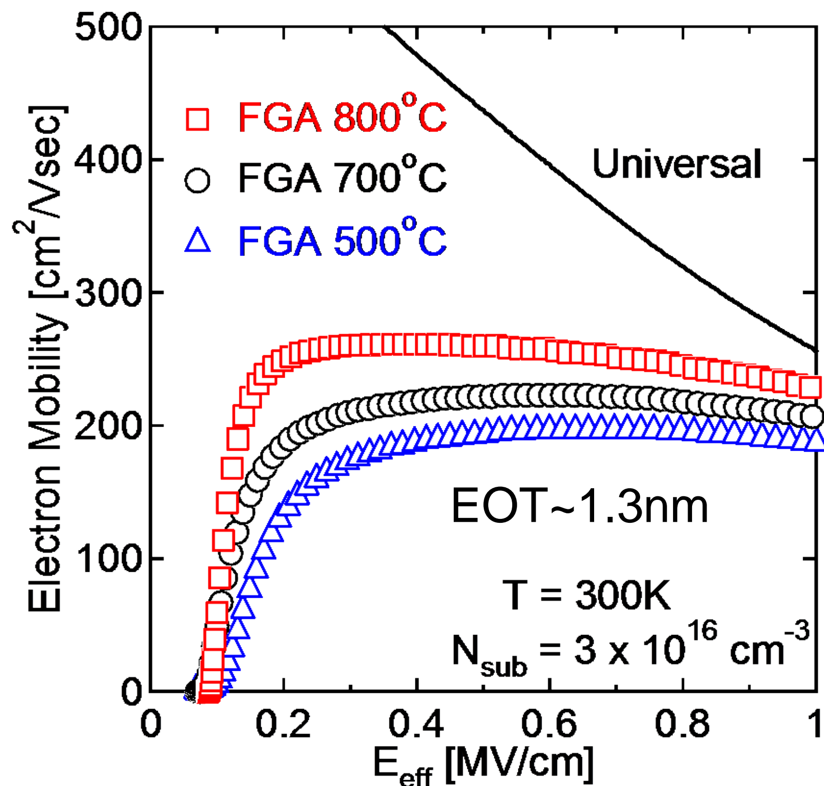


FGA800^{o}C 30min



A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)



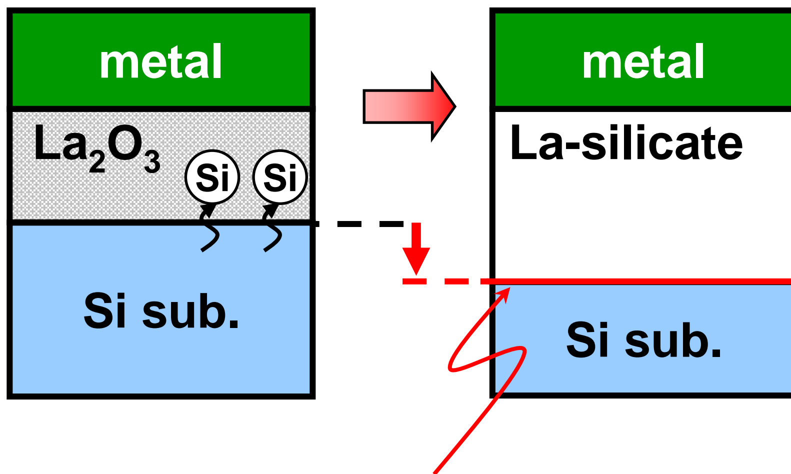


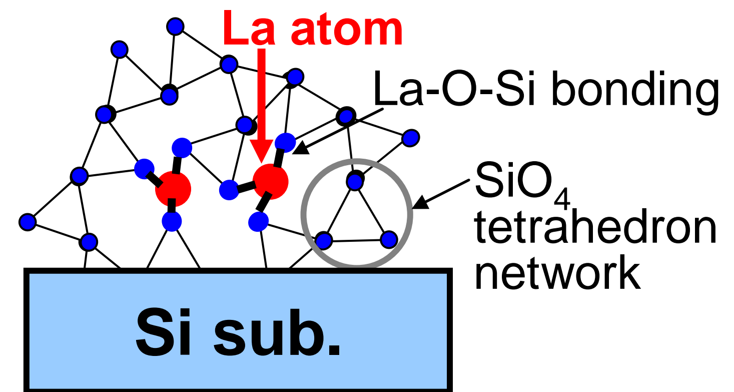
A small D_{it} of 1.6x10^{11} cm^{-2}/eV, results in better electron mobility.

Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.





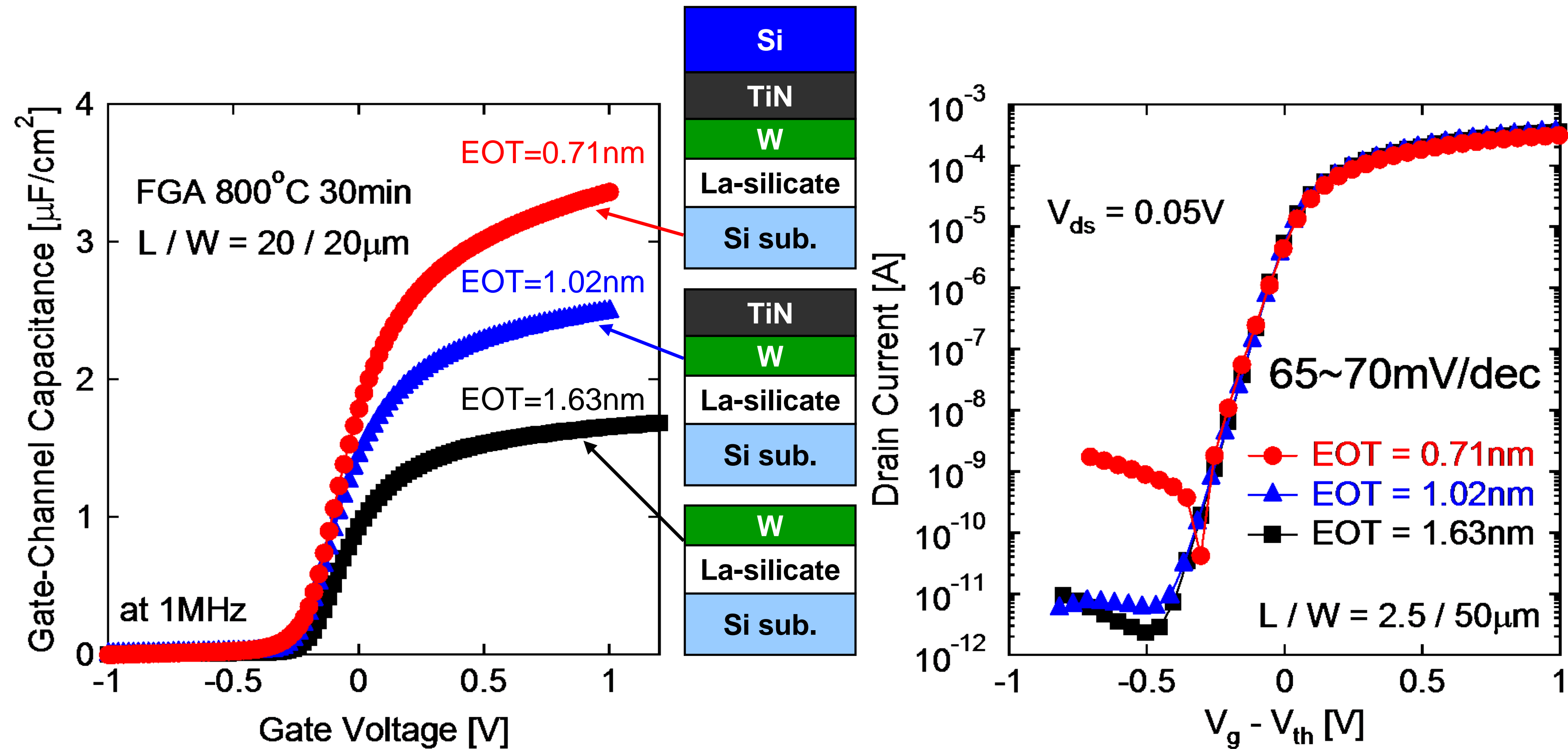
Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress

J. S. Jur, et al., Appl. Phys. Lett., Vol. 87, No. 10, (2007) p. 102908

S. D. Kosowsky, et al., Appl. Phys. Lett., Vol. 70, No. 23, (1997) pp. 3119

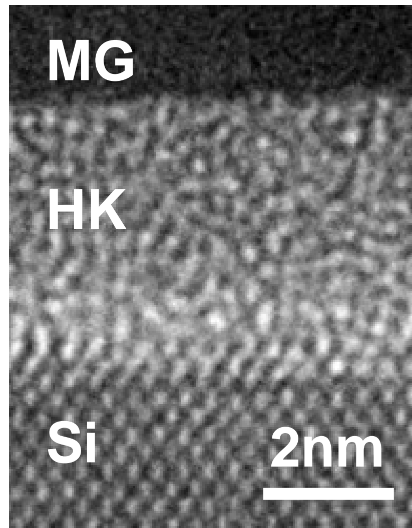
EOT growth suppression by Si coverage



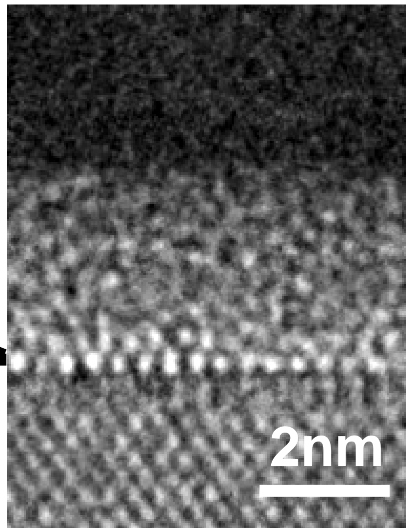
Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks

La_2O_3

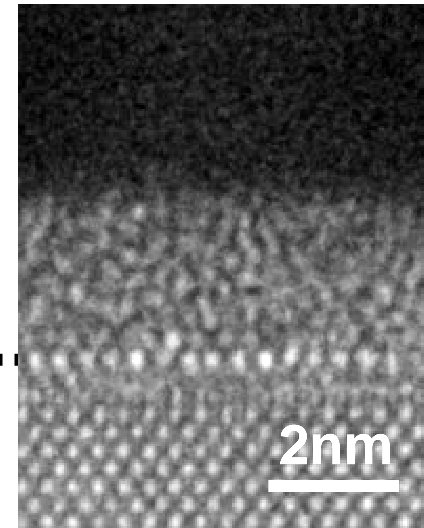
W



TiN/W



Si/TiN/W



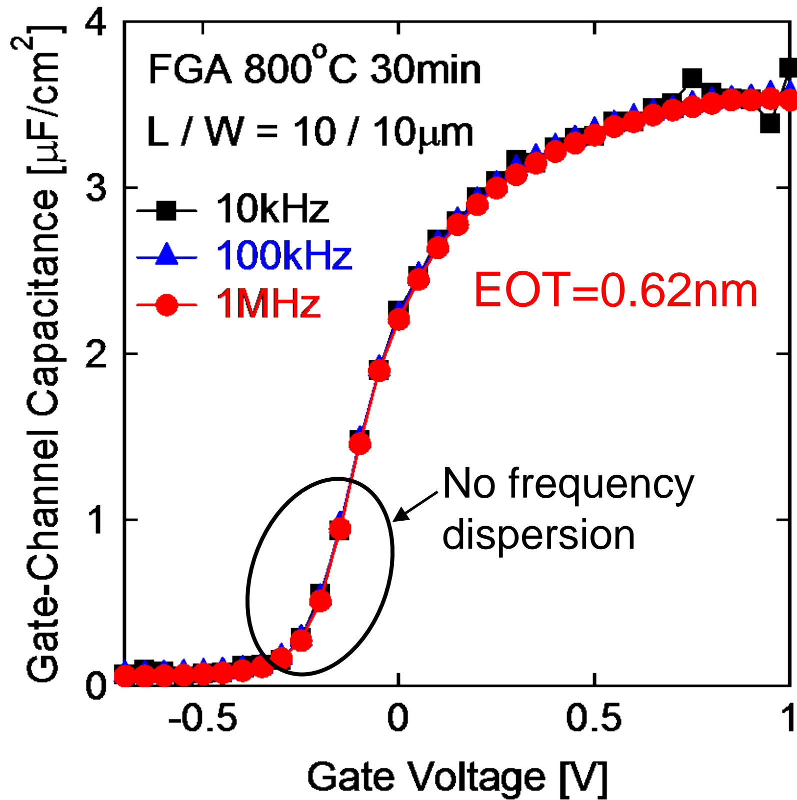
K_{av} ~ 8

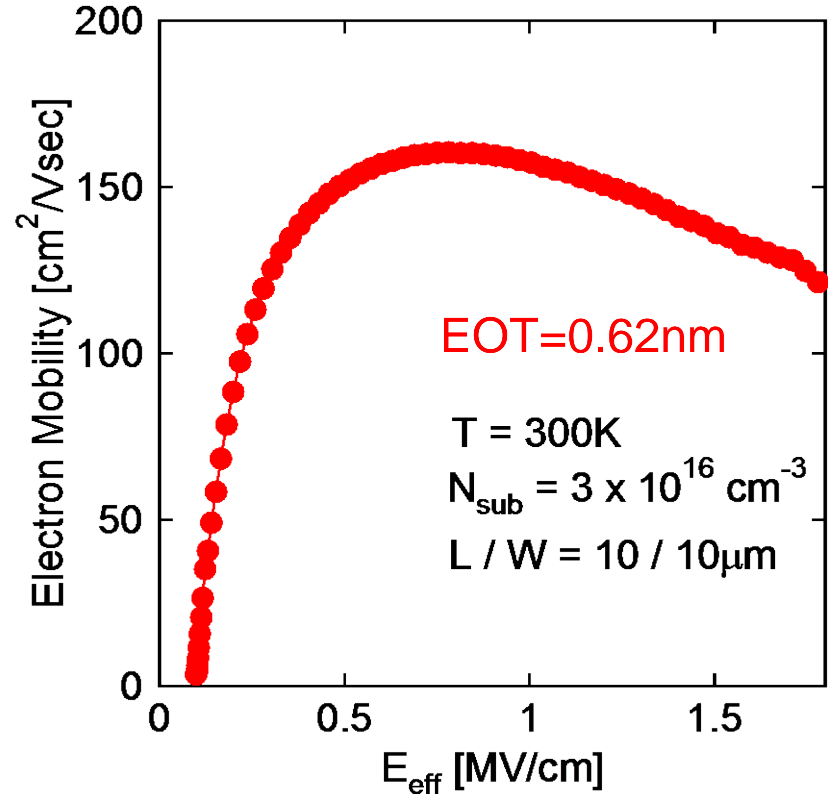
K_{av} ~ 12

K_{av} ~ 16

No interfacial layer can be confirmed with Si/TiN/W

nMOSFET with EOT of 0.62nm

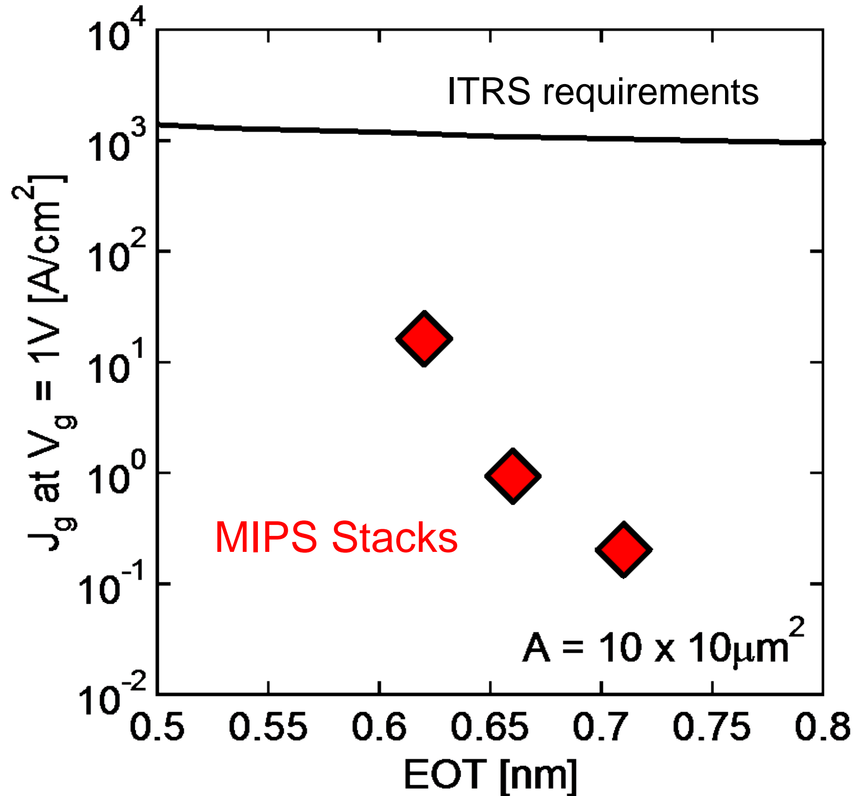


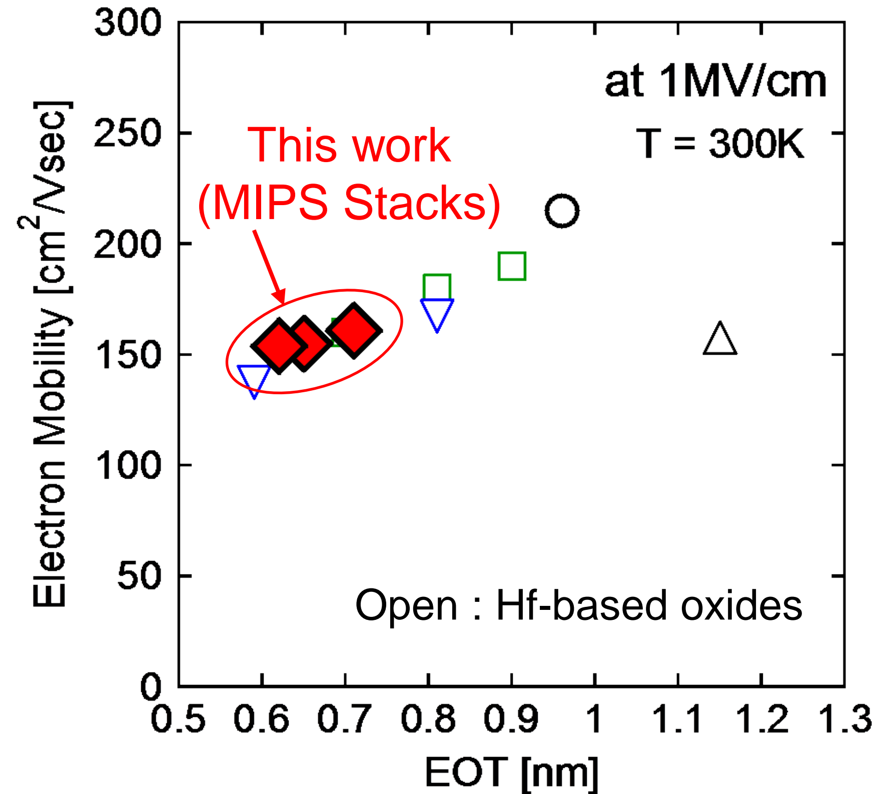


EOT of 0.62nm and 155 cm^2/Vsec at 1MV/cm can be achieved

Benchmark of La-silicate dielectrics

T. Ando et al., IEDM2009





Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides

Metal (Silicide) S/D

Extreme scaling in MOSFET

Surface or interface control

Diffusion species:

metal atom (Ni, Co)

Rough interface at silicide/Si

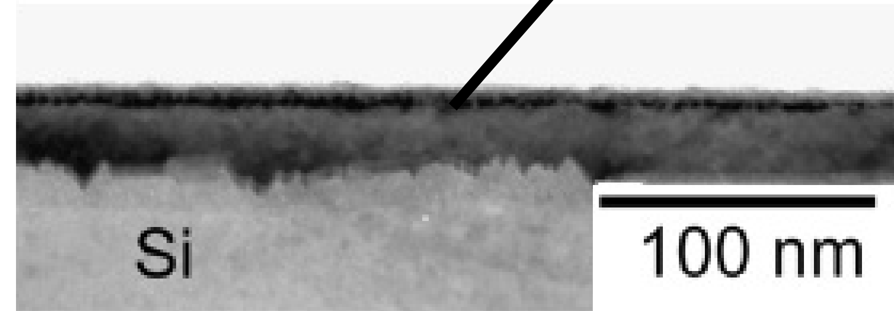
- Excess silicide formation
- Different ϕ_{Bn} presented at interface
- Process temperature dependent composition

Diffusion species: Si atom (Ti)

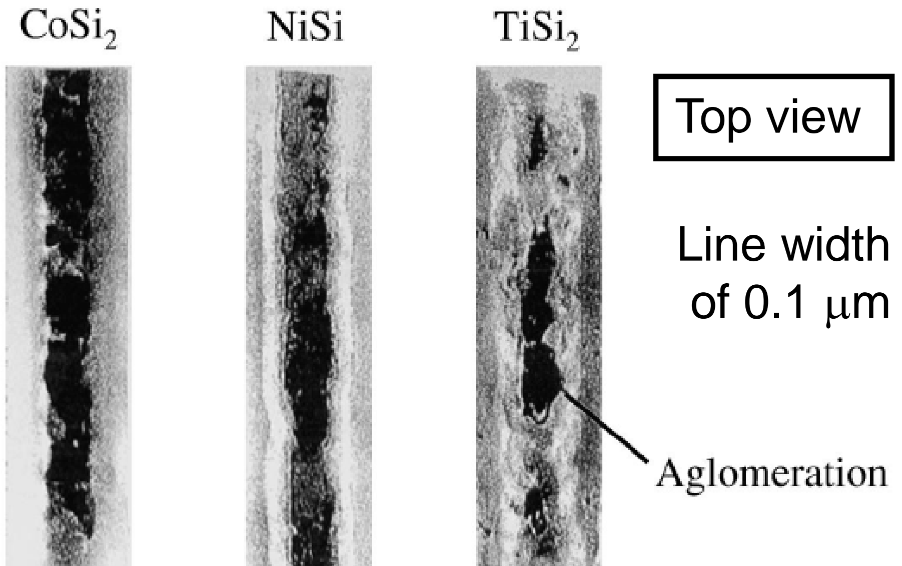
Surface roughness increases

- Line dependent resistivity change

Annealing: 650 °C



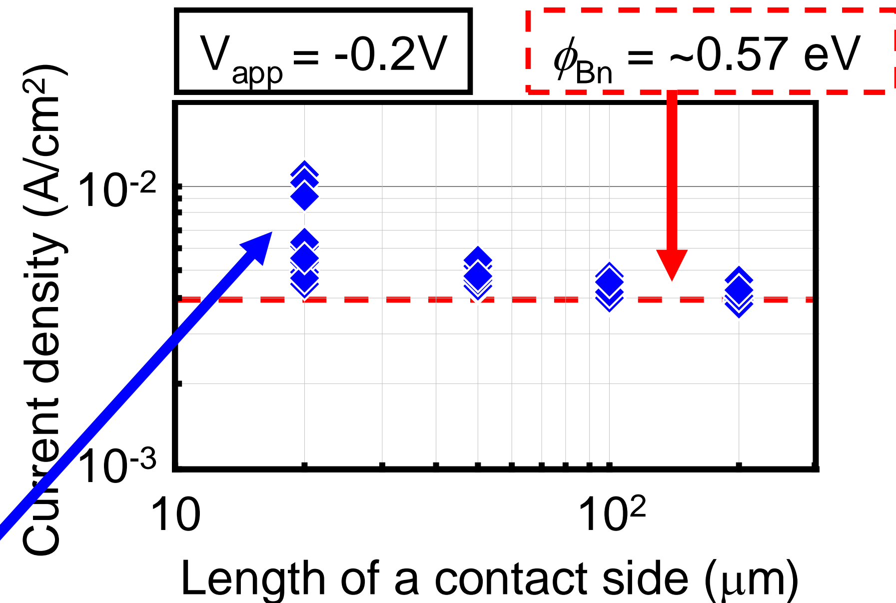
O. Nakatsuka et al., Microelectron. Eng., 83, 2272 (2006).



H. Iwai et al., Microelectron. Eng., 60, 157 (2002).

Unwanted leakage current

- Edge leakage current at periphery
- Generation current due to defects in substrate



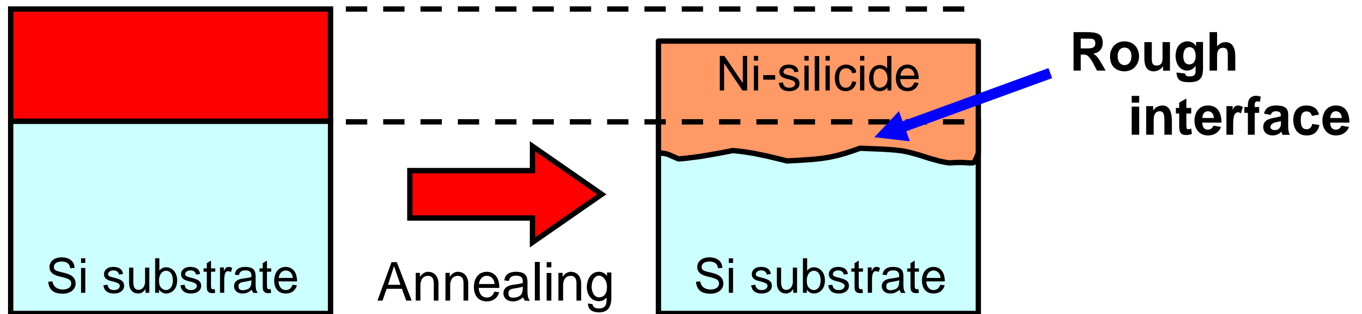
Ni silicide/Si diodes

Variable leakage current in smaller contact

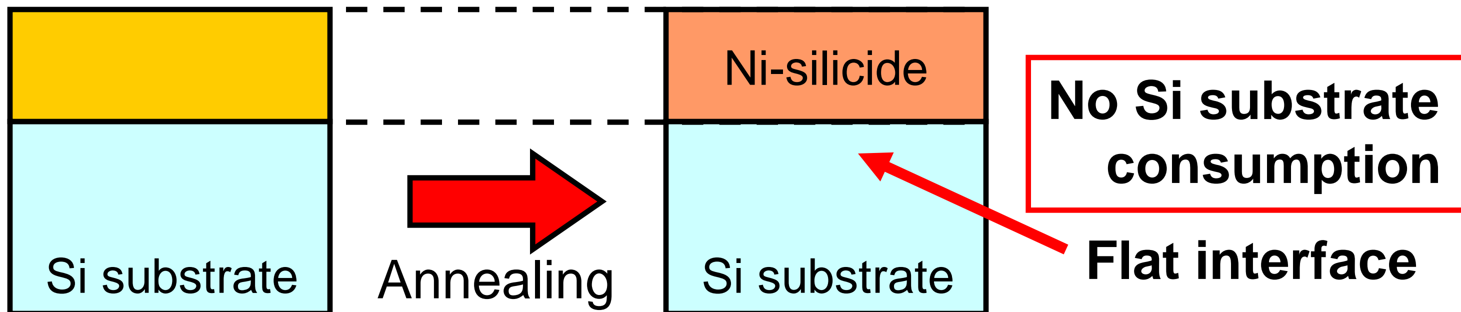
Specification for metal silicide S/D

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Deposition of Ni film



Deposition from $NiSi_2$ source

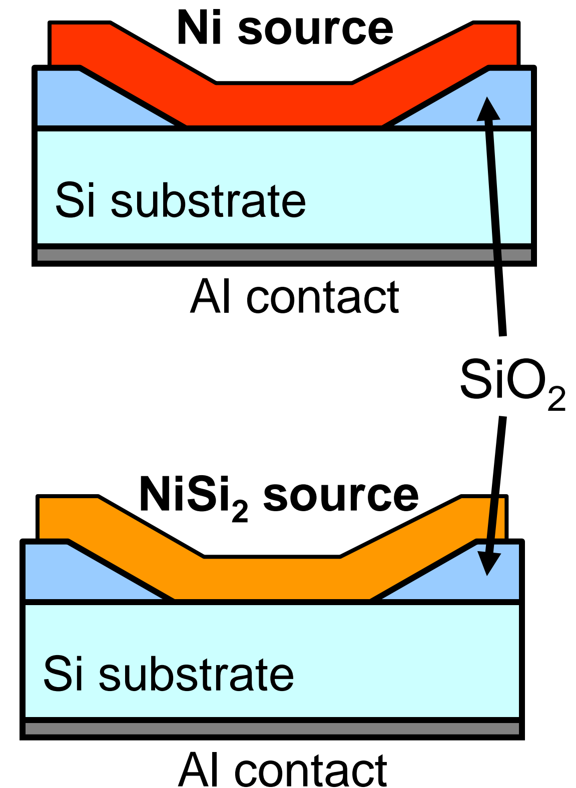


Deposition of Ni-Si mixed films from $NiSi_2$ source

- **<u>No consumption of Si atoms from substrate</u>**
- No structural size effect in silicidation process
- Stable in a wide process temperature range

- *n*-type Si substrate, Si(100) with 400 nm SiO_2 isolation
  Doping concentration : $3x10^{15}$ cm^{-3}

- SPM and HF cleaning
- Diode patterning by photolithography and BHF etching of SiO_2
- <u>Deposition of 10-nm-thick $NiSi_2$ and Ni sources by RF sputtering in Ar atmosphere</u>
- Ni silicidation by Rapid Thermal Annealing (RTA) in N_2 atmosphere
- Al contact deposition on substrate backside by thermal evaporation

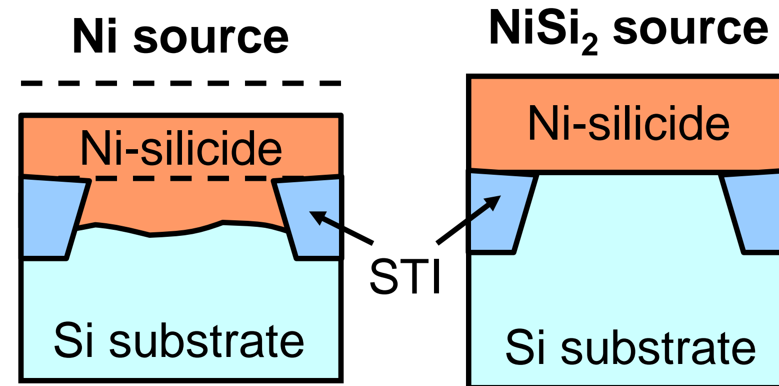


Schottky diode structures

- Measurement of electrical characteristics
- SEM and TEM observation
- XRD and XPS analysis

SEM views of silicide/Si interfaces

	Ni source (50nm)	$NiSi_2$ source (50nm)
600°C , 1min	STI, rough, 500nm	STI, flat, 500nm
700°C , 1min	STI, rough, 500nm	STI, flat, 500nm
800°C , 1min	STI, rough, 500nm	STI, flat, 500nm

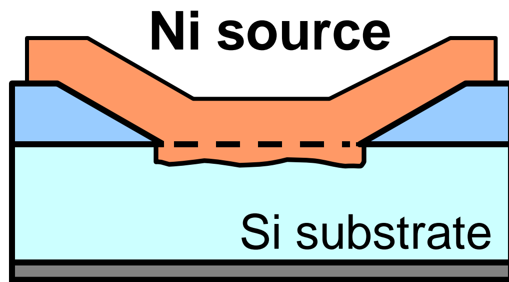


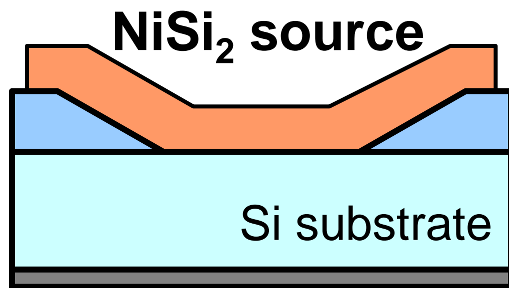
Ni source

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

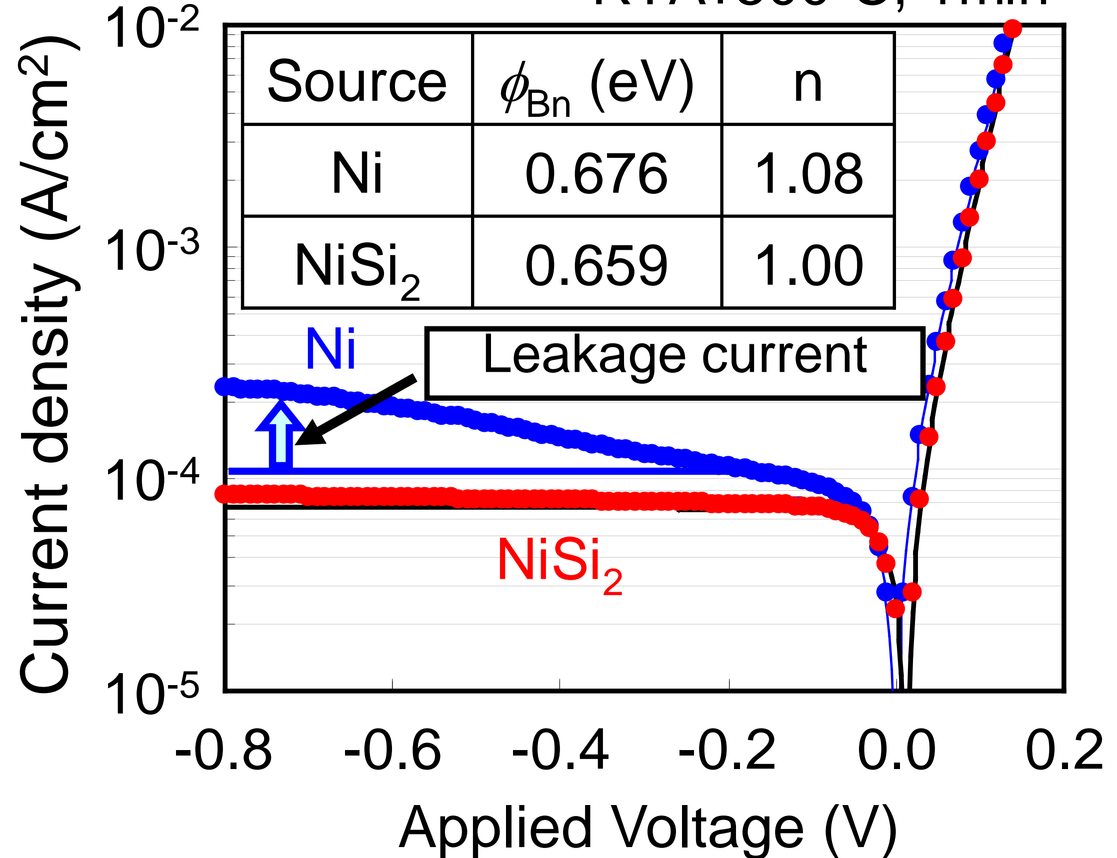
$NiSi_2$ source

- **Atomically flat interfaces**
- **No Si consumption**
- Temperature-independent





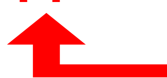
Schottky diode structures



NiSi$_2$ source

Ideal characteristics (n = 1.00, suppressed leakage current)

Suppressed reverse leakage current

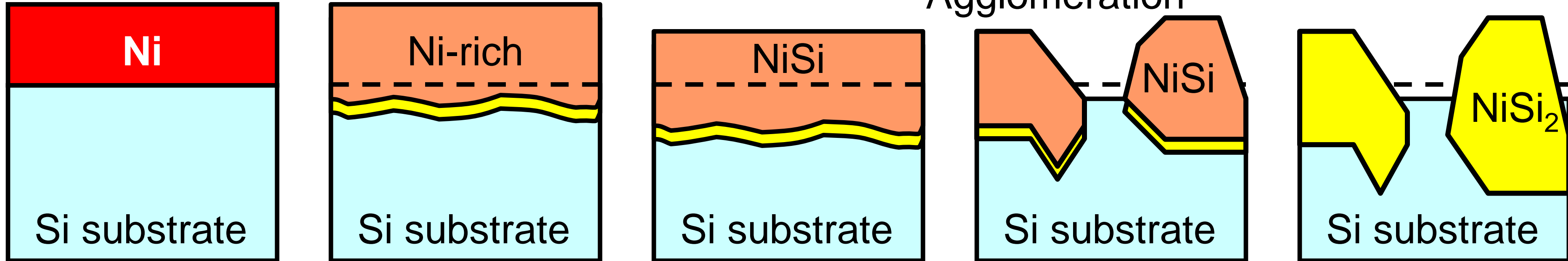


- Flat interface and No Si substrate consumption
- No defects in Si substrate

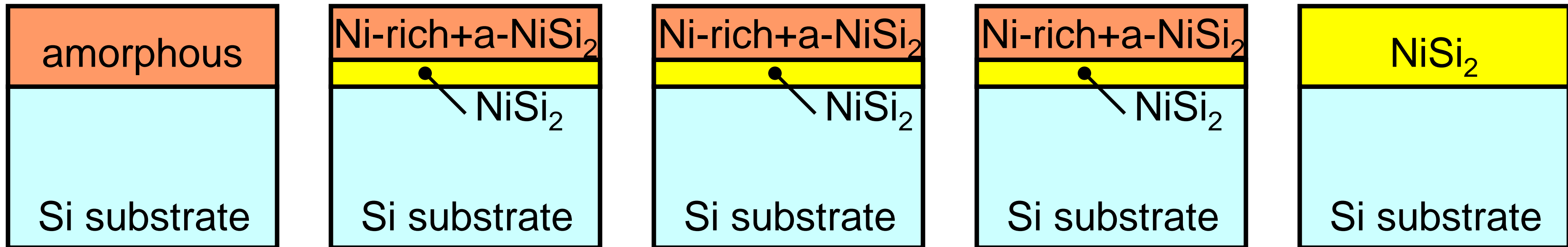
as-deposited → 300°C → 550°C → 800°C

Ni source

Agglomeration



$NiSi_2$ source

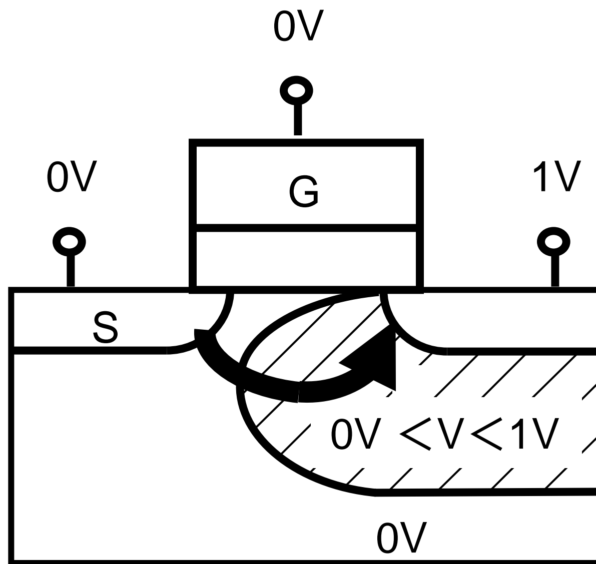


- Ni-rich phases in the silicide layer are maintained with $NiSi_2$ source

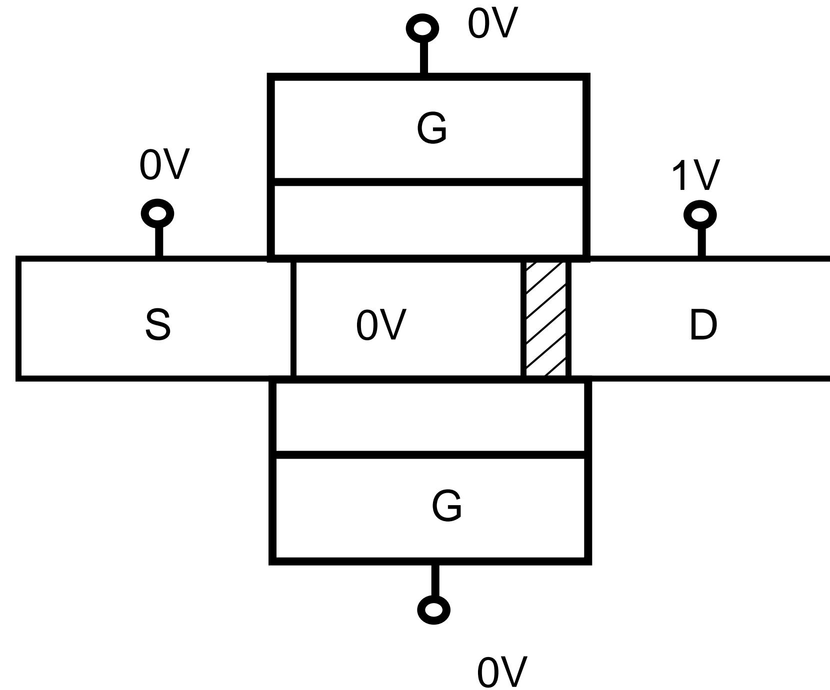
- No distinct structure change at the interface
  → **Stable ϕ_{Bn} and *n*-factor**
  → **No structural effect for silicidation**

Wire channel

Suppression of subthreshold leakage by surrounding gate structure



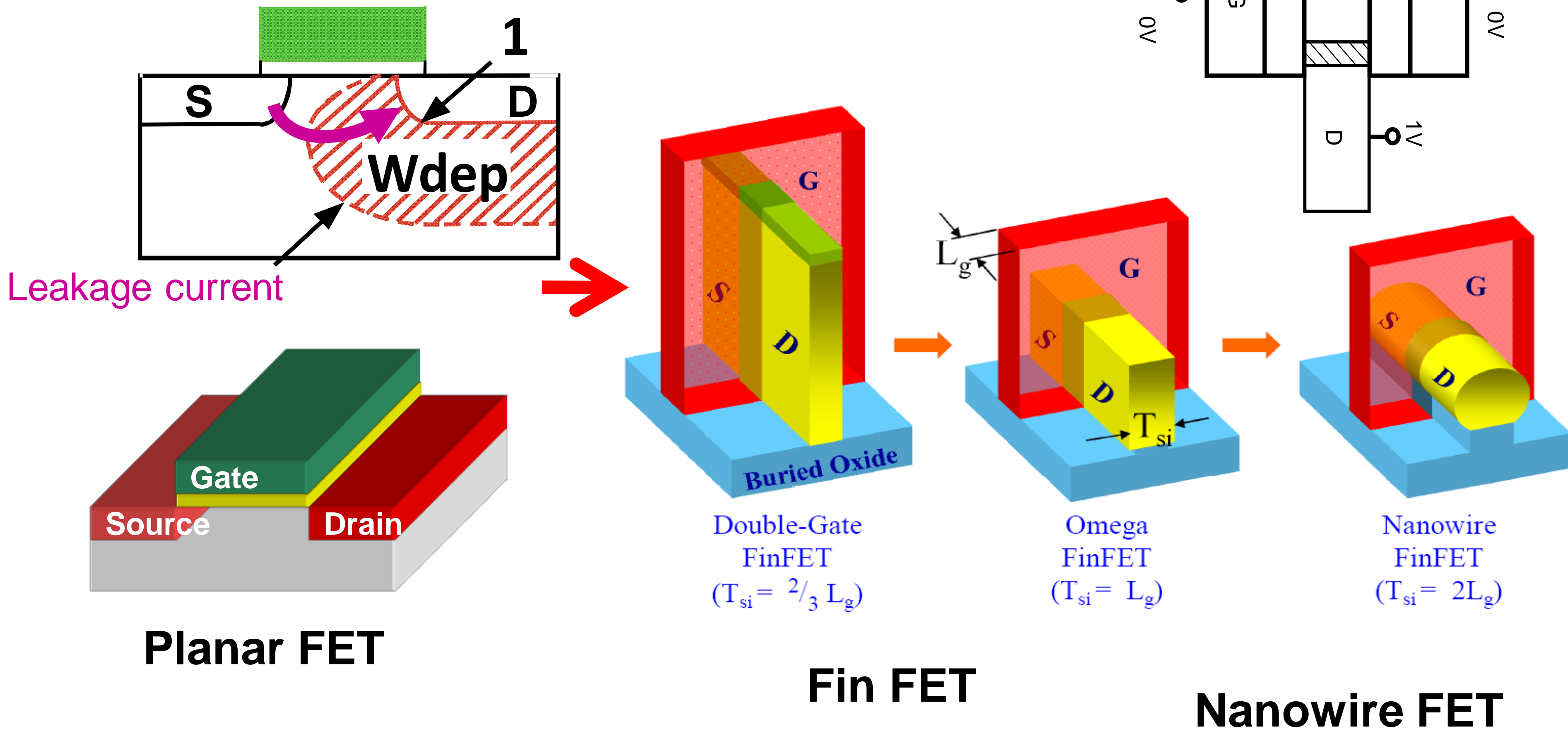
Planar



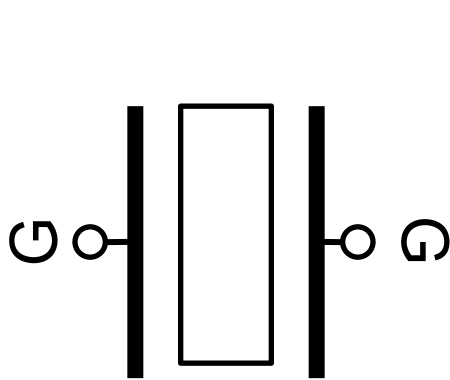
Surrounding gate

Because of off-leakage control,

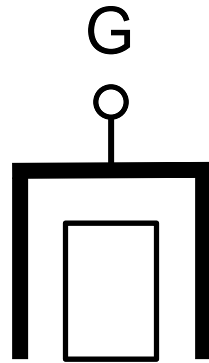
Planar → Fin→ Nanowire



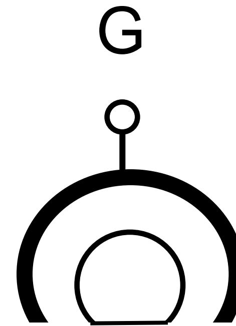
Nanowire structures in a wide meaning



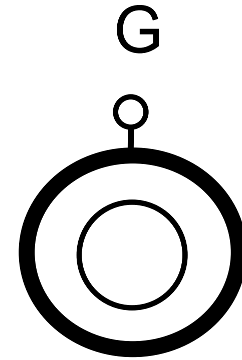
Fin



Tri-gate



Ω-gate



Nanowire

Nanowire FET

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Device Structures																
Planar bulk																
FDSOI																
Multiple Gate																

2015

22 or 16nm node

Multiple Gate (Fin) FET

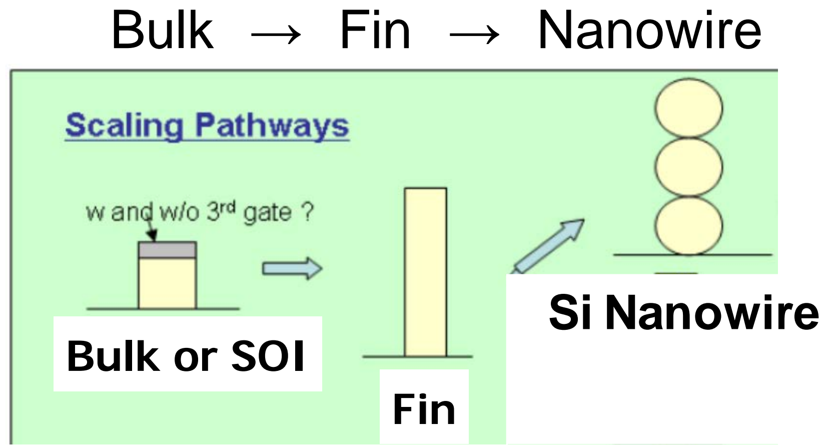
2020

11 or 8nm node

Nanowire FET

ITRS 2009

Bulk → Fin → Nanowire

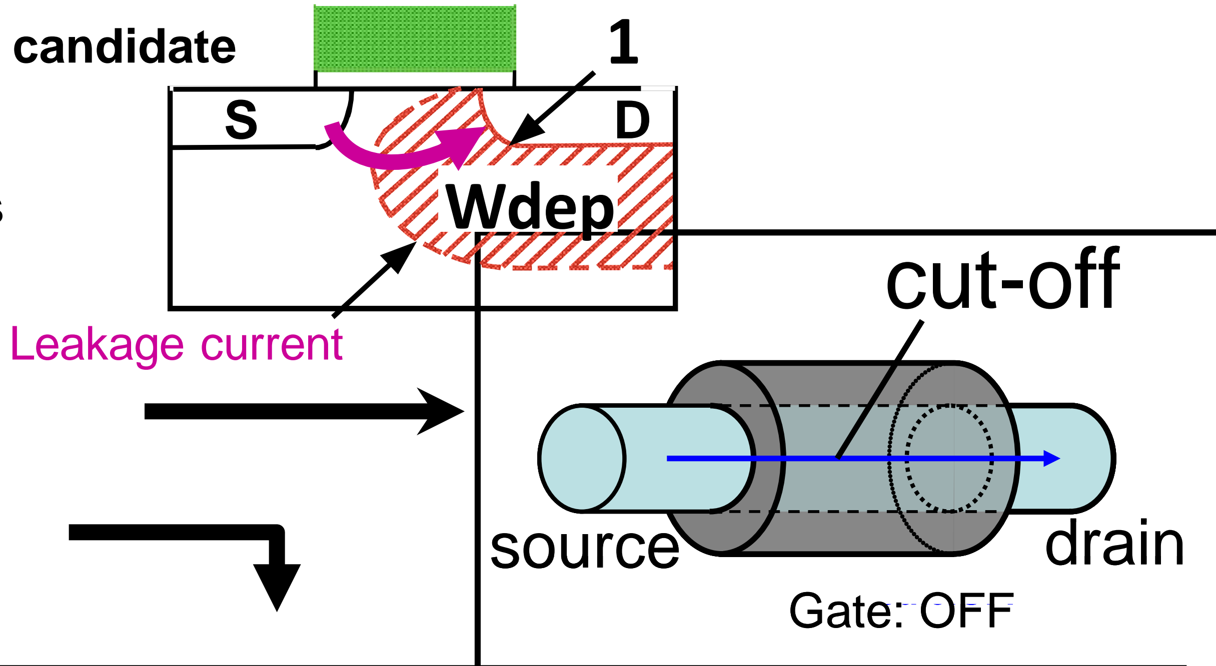


Si nanowire FET as a strong candidate

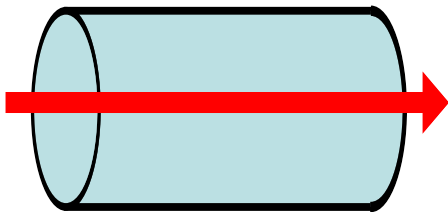
1. Compatibility with current CMOS process

2. Good controllability of I_{OFF}

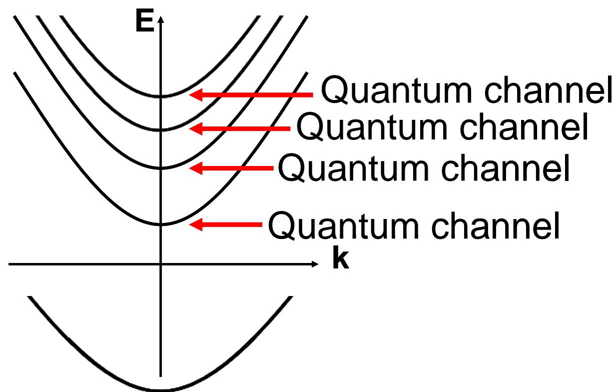
3. High drive current



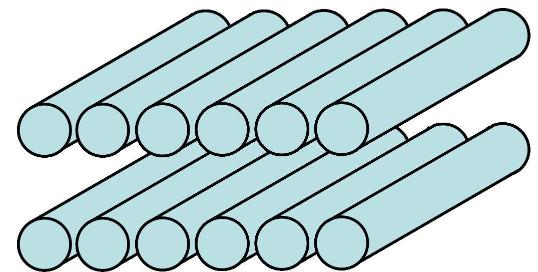
1D ballistic conduction



Multi quantum Channel

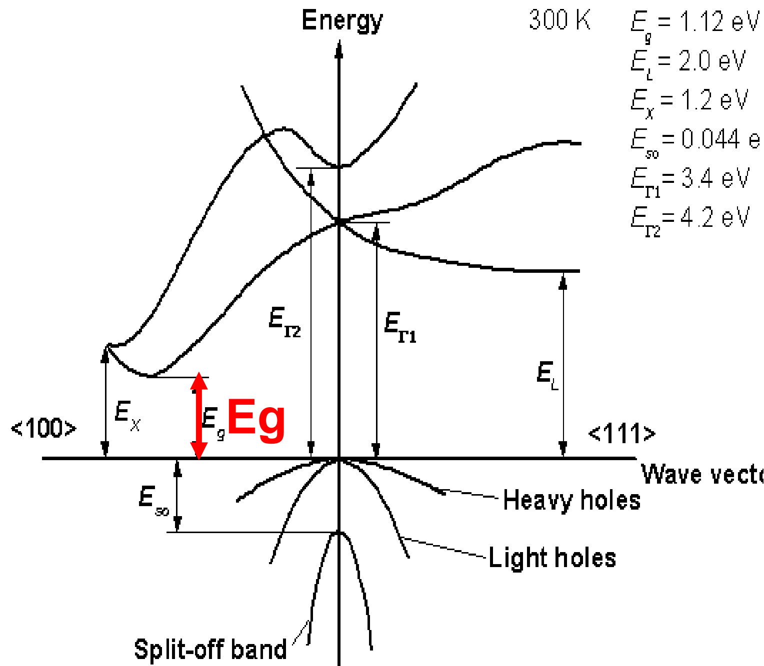


High integration of wires

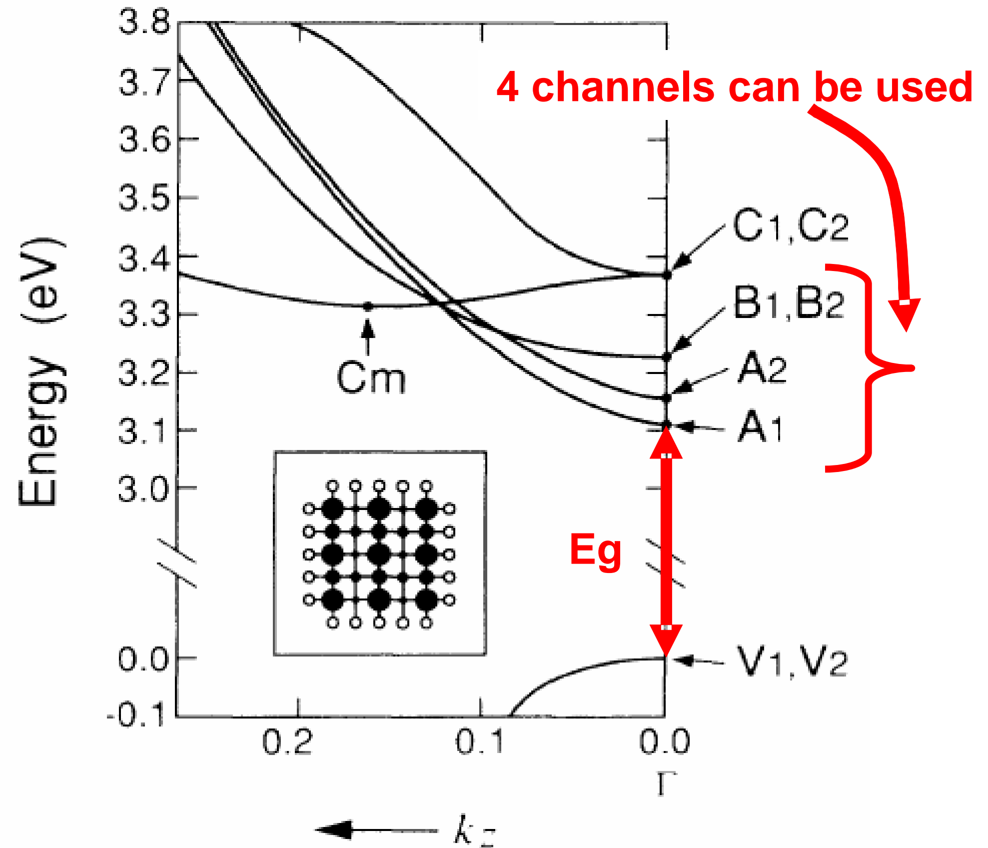


Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



Energy band of Bulk Si



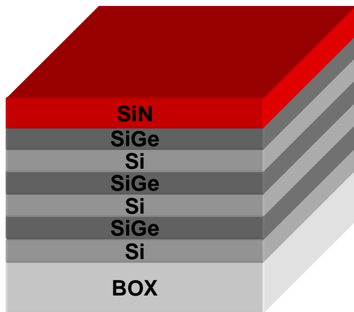
Energy band of 3 x 3 Si wire

Device fabrication

$Si/Si_{0.8}Ge_{0.2}$
superlattice
epitaxy on SOI

Anisotropic
etching
of these layers

Isotropic
etching
of SiGe

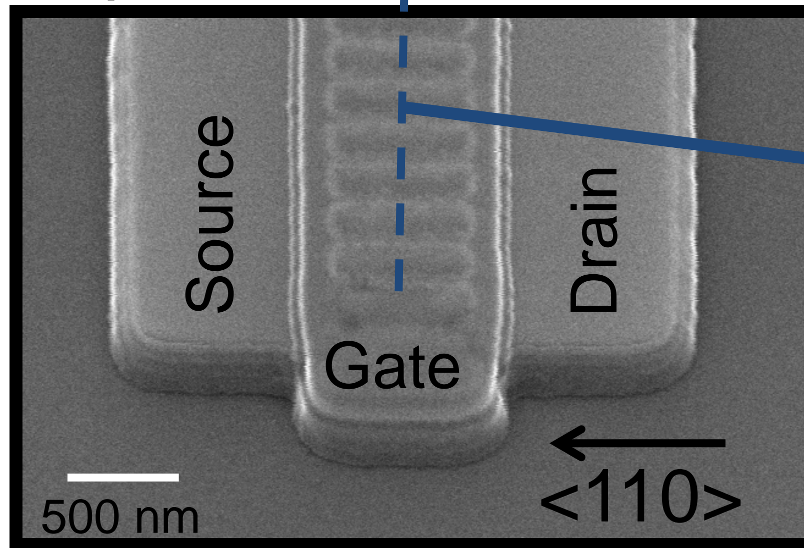


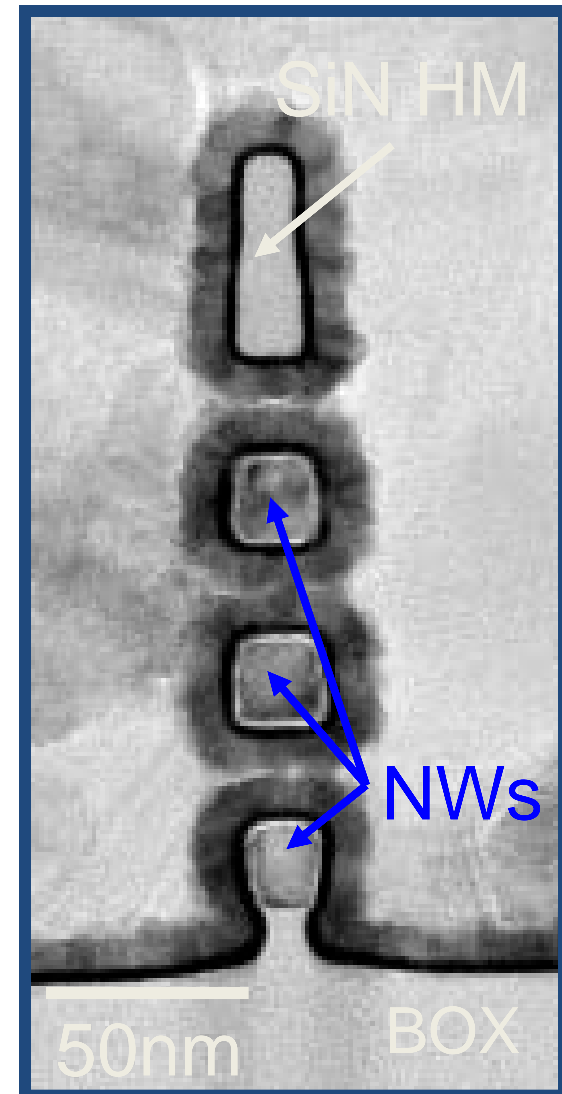
Gate depositions

S/D implantation
Spacer formation
Activation anneal
Salicidation

3D-stacked Si NWs with Hi-*k*/MG

Top view

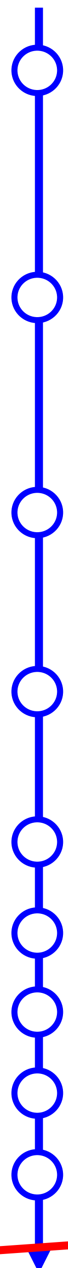




Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

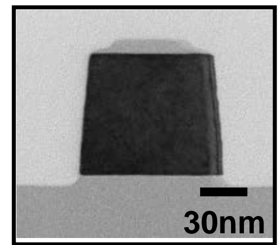
C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

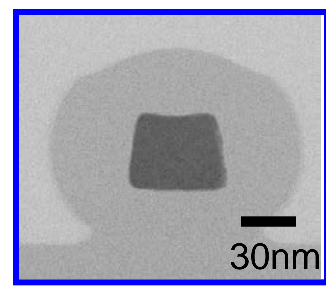
SiNW FET Fabrication

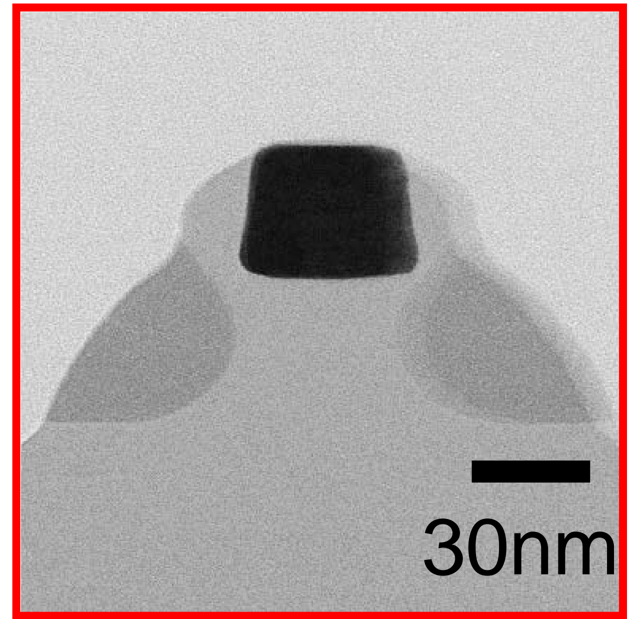


- S/D & Fin Patterning
- Sacrificial Oxidation
- Oixde etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

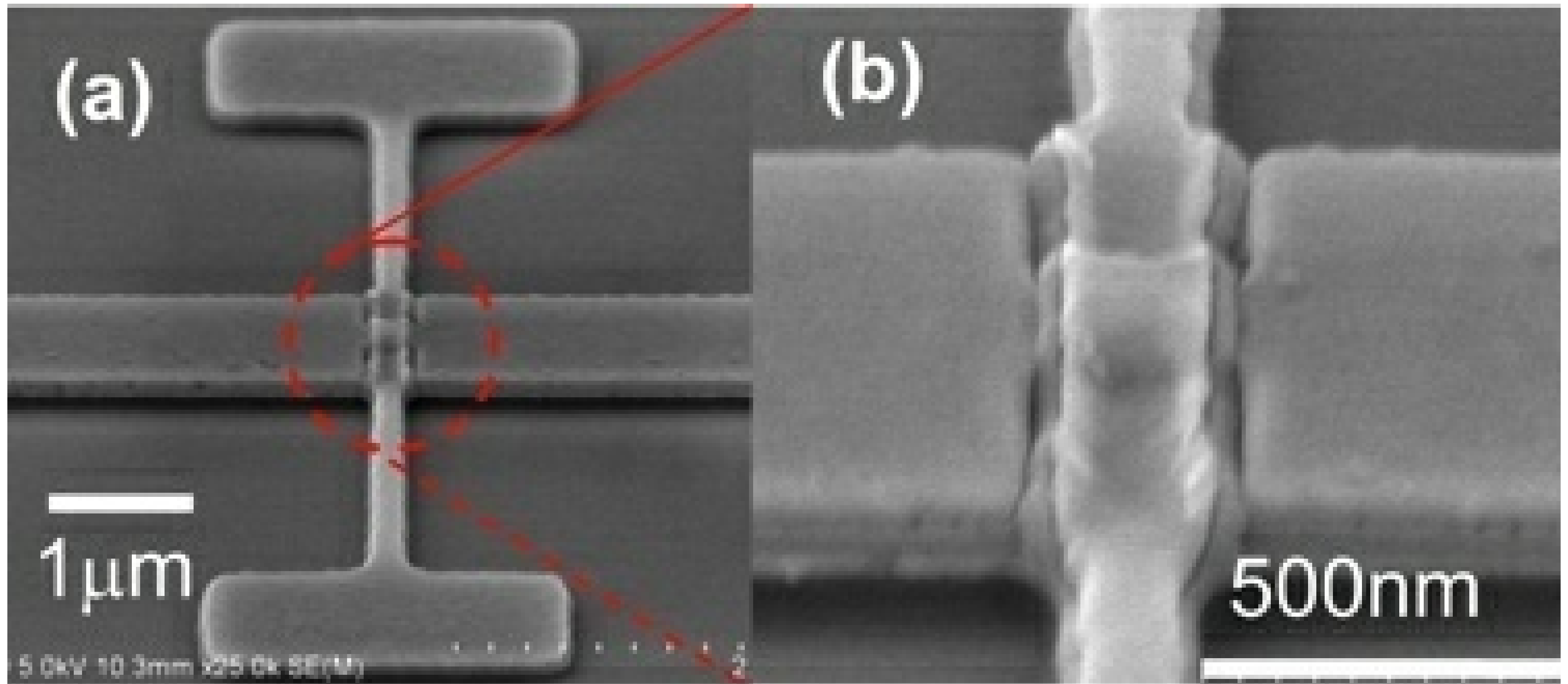
Standard recipe for gate stack formation





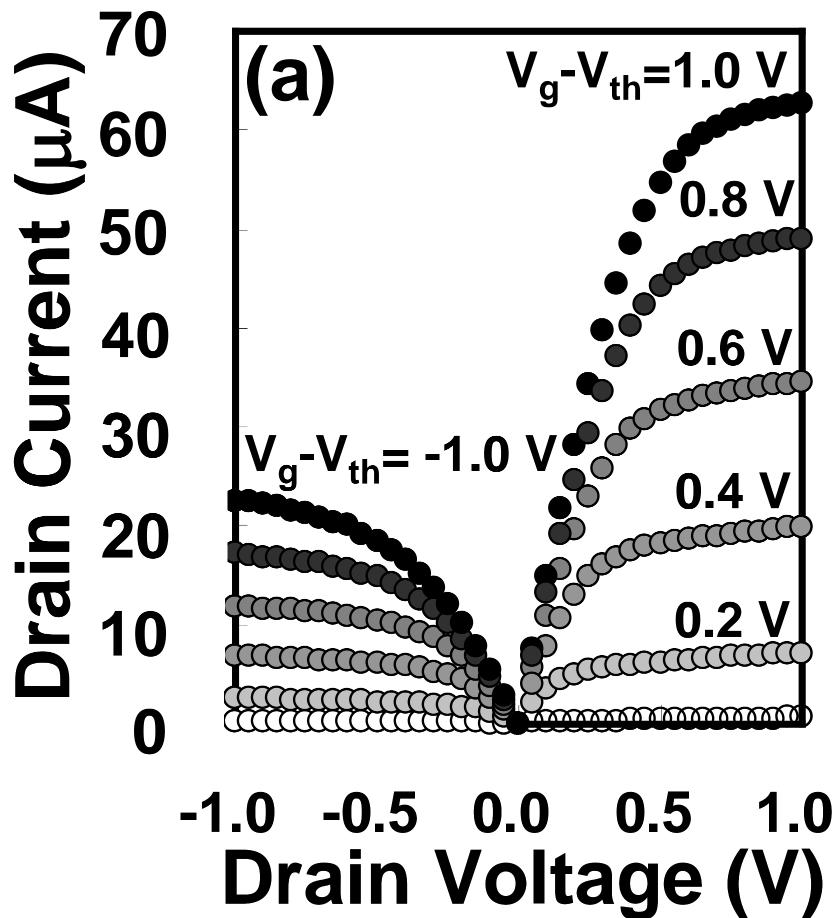


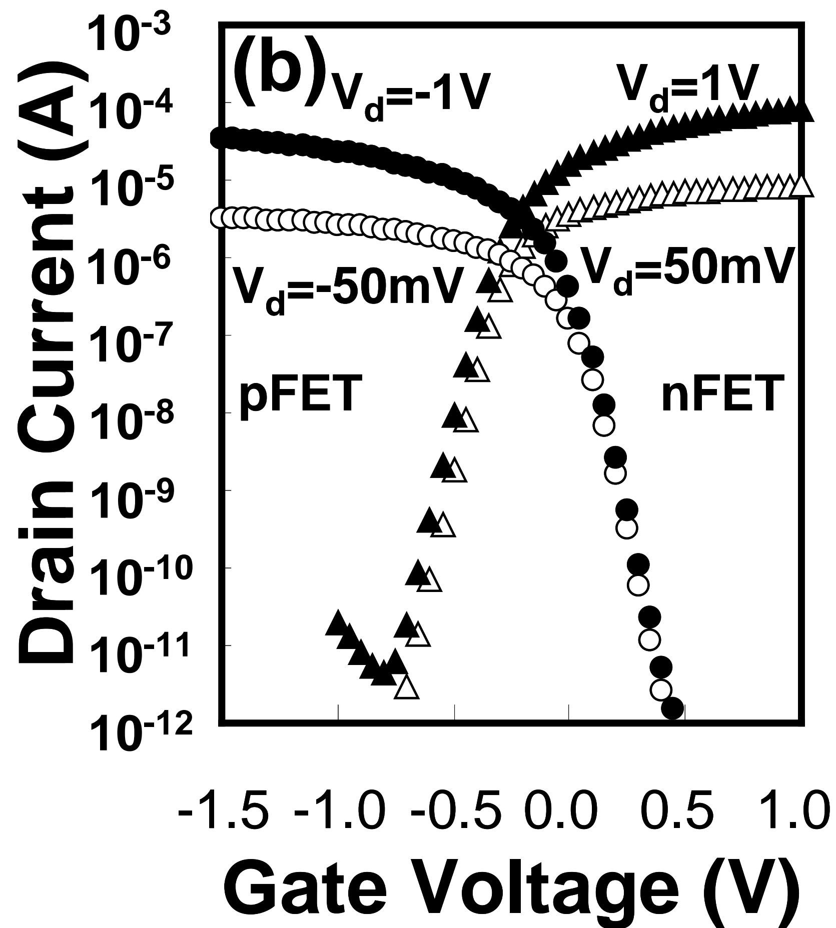
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



Recent results to be presented by ESSDERC 2010 next week in Sevile

Wire cross-section: 20 nm X 10 nm

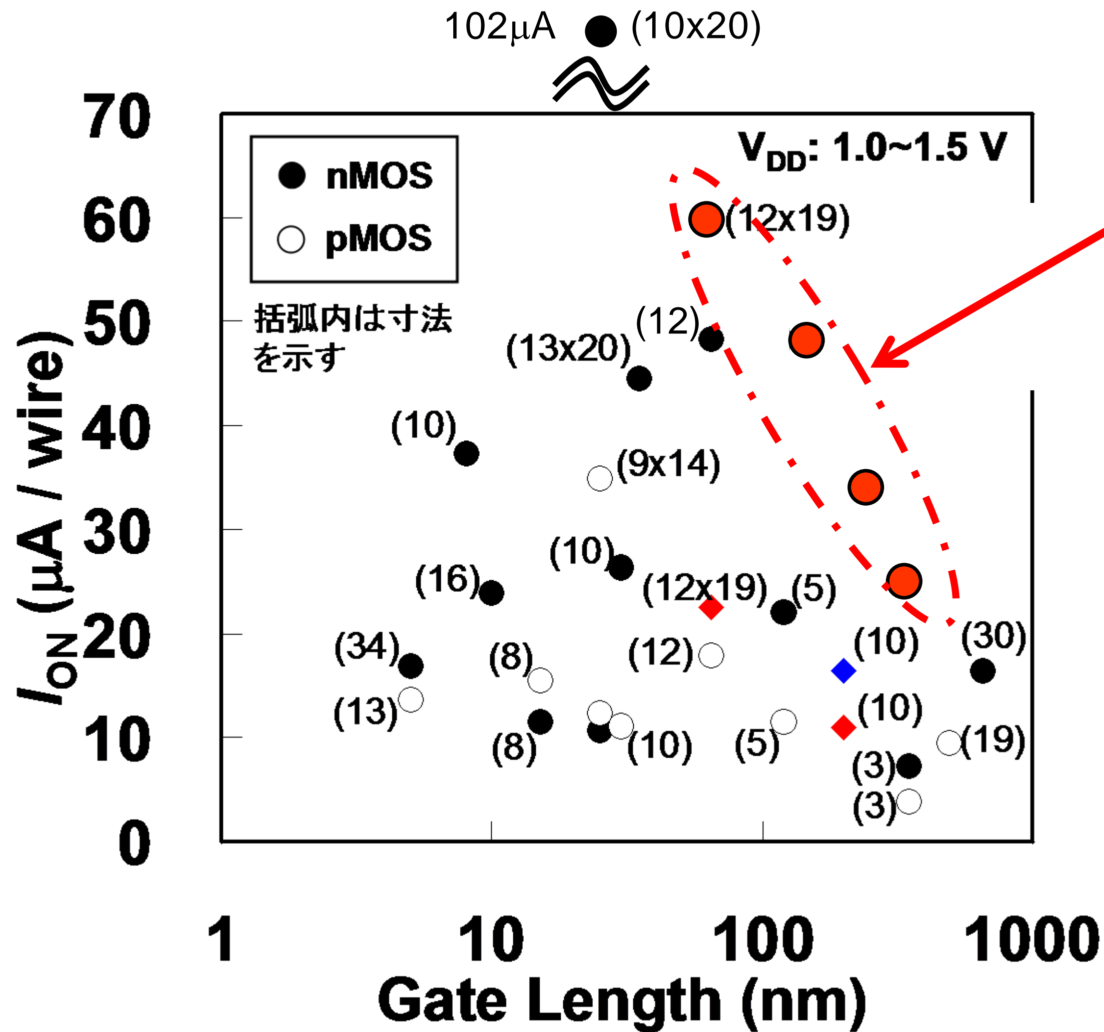




On/Off>10^6、60uA/wire

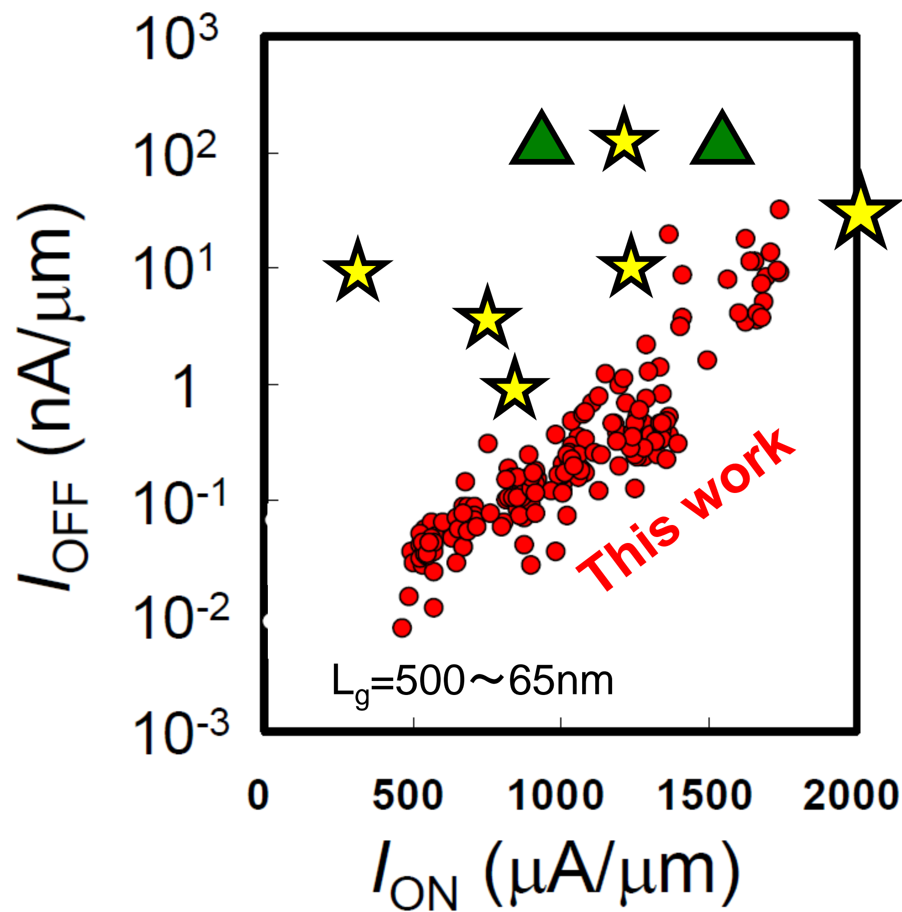
L_g=65nm, T_{ox}=3nm

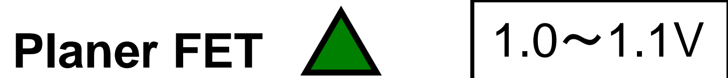
Bench Mark



Our Work

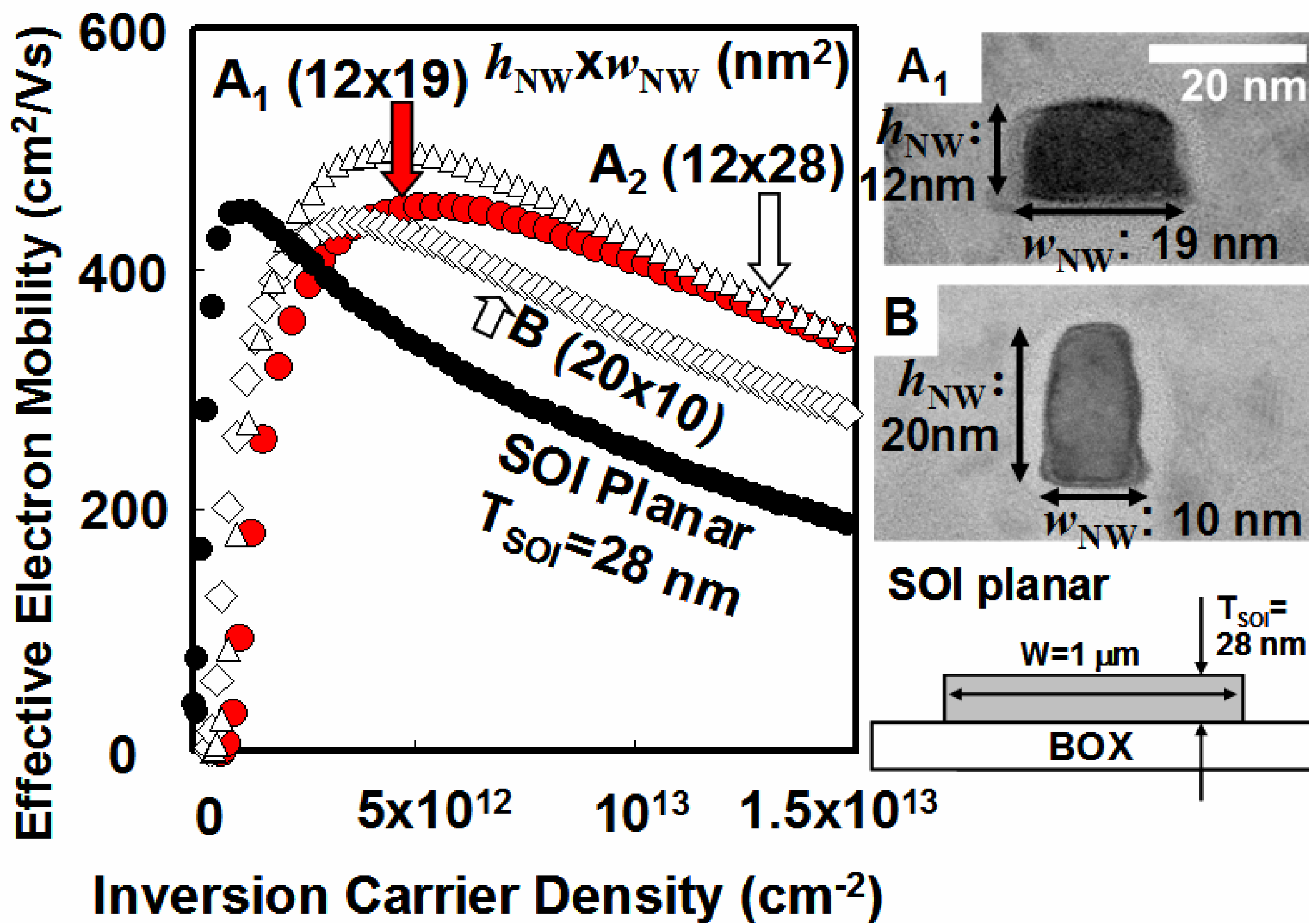
I_{ON}/I_{OFF} Bench mark

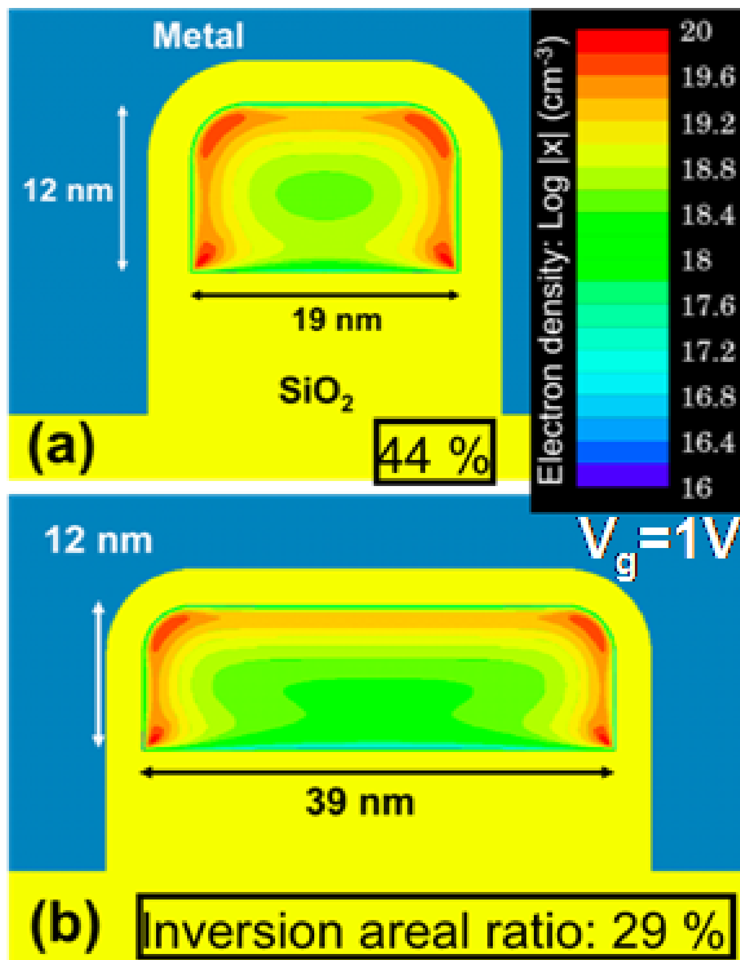




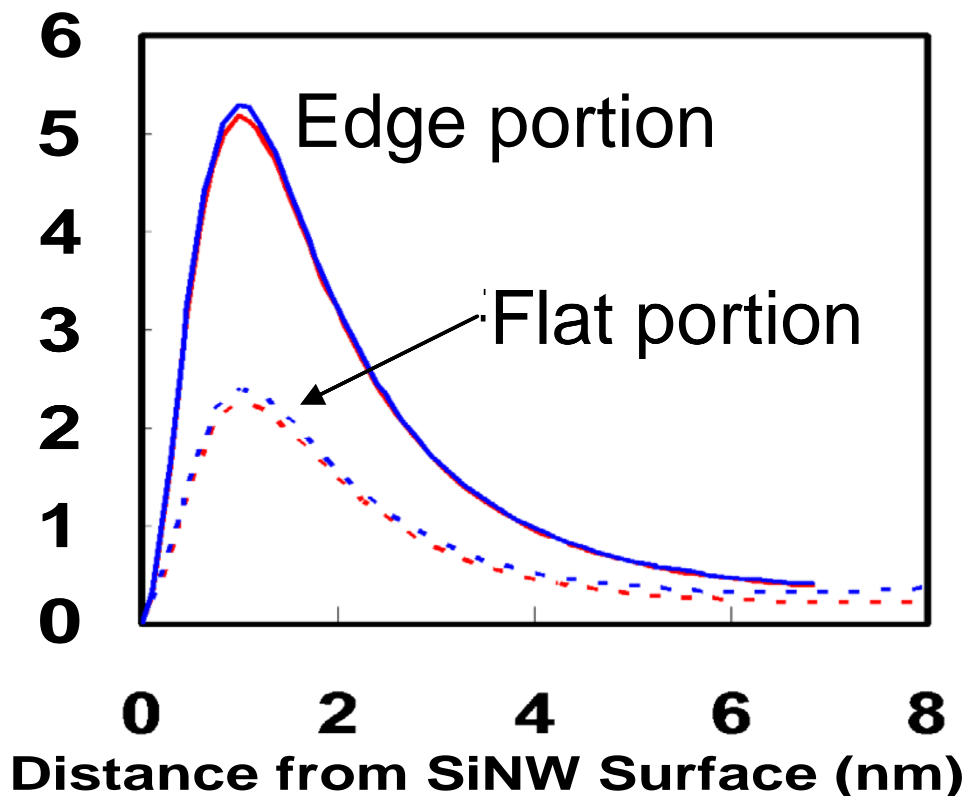
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240


Effective Electron Mobility (cm²/Vs)
600
400
200
0
A1 (12x19)
hNWxwNW (nm²)
A2 (12x28)
B (20x10)
SOI Planar
TSOI=28 nm
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
A1
20 nm
hNW:
12nm
wNW: 19 nm
B
hNW:
20nm
wNW: 10 nm
SOI planar
TSOI=
28 nm
W=1 µm
BOX



Metal
12 nm
19 nm
SiO_2
(a)
44 %
Electron density: Log |x| (cm-3)
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
V_g=1V
12 nm
39 nm
(b)
Inversion areal ratio: 29 %

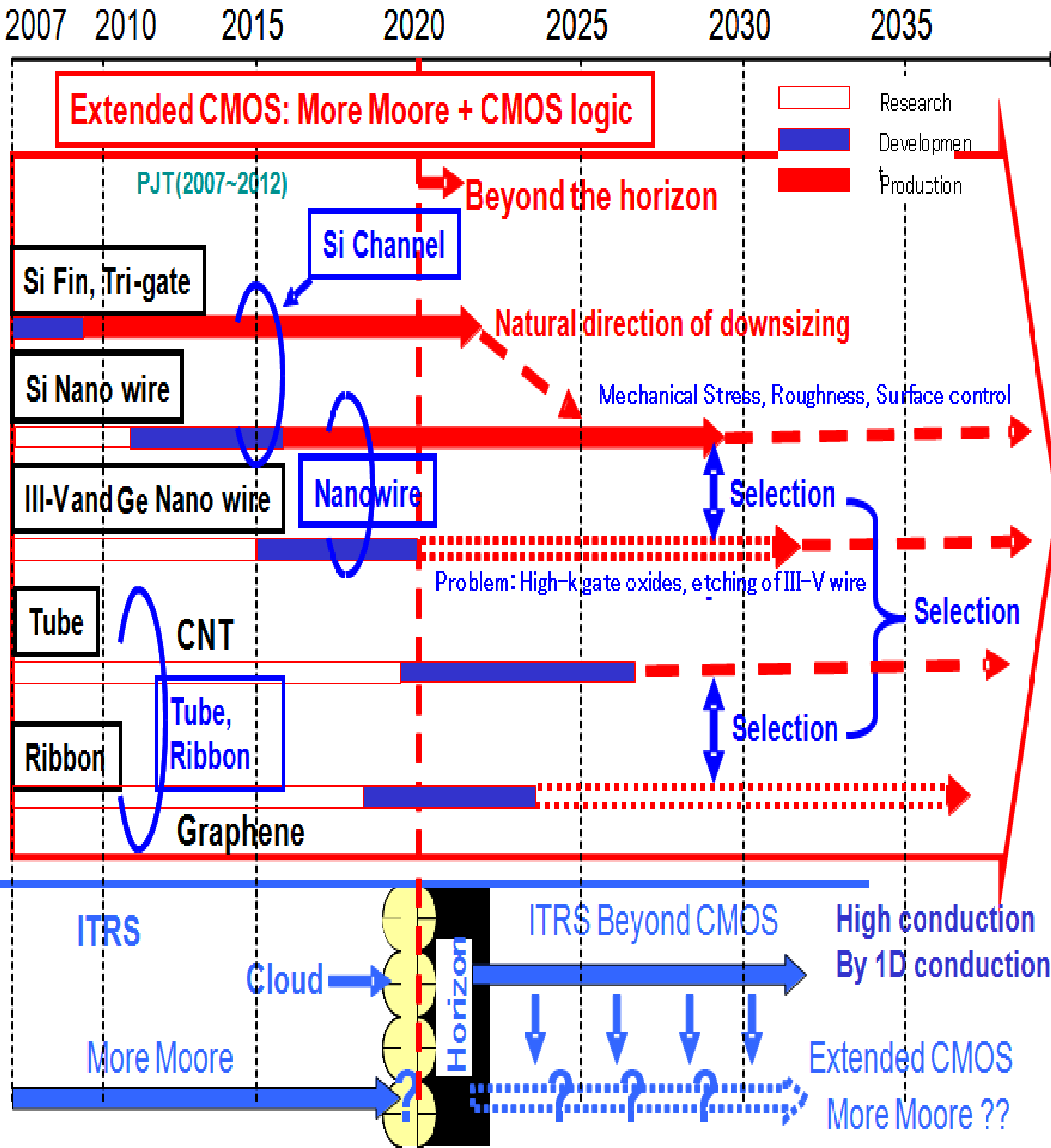


Electron Density
($x10^{19}cm^{-3}$)
Edge portion
Flat portion
0
1
2
3
4
5
6
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !

Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you
for your attention!